NEW TECHNICAL THEORY
FOR SERVICING

DTC-55ES

OPERATION MANUAL

DIGTAL AUDIO TAPE DECK

SONY

1. OUTLINE

The DTC-55ES is the first Sony DAT deck incorporating a new standard (named SCMS) which allows to record digital signals of the first generation from digital sources such as CD.
The unit has many new features which the predecessor lacked such as the long play (LP) mode and a vertically see-through mechanism.
A newly developed IC has been included in the signal processing circuit, viz. a servo MICON circuit which greatly simlifies the circuitry.

1-1. Main Features

1) Complies with the Serial Management System (SCMS) which proves very useful for regulating direct digital copying from CD.
2) The unit has a high-precision mechanism with a vertical see-through cassette compartment
3) Long playing is made possible by adopting second-generation LSI. The following modes exist : 48k (standard mode), 44k/32k mode (option 1) which both allow maximum 120 minutes of recording and playback ; 32k LP mode (option 2) which is capable of maximum 240 minutes of recording/playback.
   Table 1-1 shows some examples of inputs and sources.
4) The digital fade in/out feature allows to set the digital input and the analog input/output between 0.2 - 15 seconds.
5) The fs map feature enables to display the sampling frequency with the recorded tape is copied.
6) The A/D-D/A monitor operation allows to monitor the digital input signal through D/A conversion. It is also possible to monitor analog inputs by A/D-D/A conversion.

Table 1-1

	Max : REC TIME	Sampling frequency	Digitalized Bit	Input Sources.
48k mode (Standard)	120min.	48kHz	16bit linear	digital (Dat. Satellite Boardcasting B mode)
				analog (Source in general)
32k mode (Option 1)	120min.	32kHz	16bit linear	digital (Satellite Broadcasting A mode)
32k LP mode (Option 2)	240min.	32kHz	12bit non-linear	digital (Satellite Broadcasting A mode)
				analog (Source in general)
44k mode	120min.	44kHz	16bit linear	digital (CD)

* In the case of digital inputs, the mode is selected automatically by the digital signal's sampling frequency. However, two options are possible in the 32k mode.

* In the case of analog input, both the 48k and the 32k LP can selected regardless of the input source.

Table 1-2 Main Dat Specifications (DTC-55ES)

Item \ Mode	REC/PB mode				Pre-recorded tape (PB only)
	(48k mode)	(32k mode)	(32k-LP mode)	(44k mode)	(44k-WT mode)
Channel number (CH)	2	2	2	2	2
Sampling frequency (kHz)	48	32	32	44.1	44.1
Quantization bit number (bit)	16 (Linear)	16 (Linear)	12 (Non-Linear)	16 (Linear)	16 (Linear)
Transmission rate (MBPS)	2.46	2.46	1.23	2.46	2.46
Sub-code capacity (MBPS)	273.1	273.1	136.5	273.1	273.1
Modulation System	8-10 conversion				
Correction System	Double Reed-Solomon code				
Tracking System	Area Sharing ATF				
Cassette Size (mm)	73 × 54 × 10.5				
Recording Time (min)	120	120	240	120	80
Tape width	3.81				
Tape type	Metal powder				Dxide tape
Tape Thickness (μm)	13 ± 1μ				
Tape Speed (mm/s)	8.15	8.15	4.075	8.15	12.225
Track pitch (μm)	13.591				20.41
Track angle	6° 22′ 59.5″				6° 23′ 29.4″
Standard drum specifications	ϕ 30 90° Wrap				
Drum rotations (rpm)	2,000		1,000	2,000	2,000
Relative Speed (ϕ = 30) (m/s)	3.133		1.567	3.133	3.129
Head azimuth angle	± 20°				

2. OVERALL CONSTRUCTION

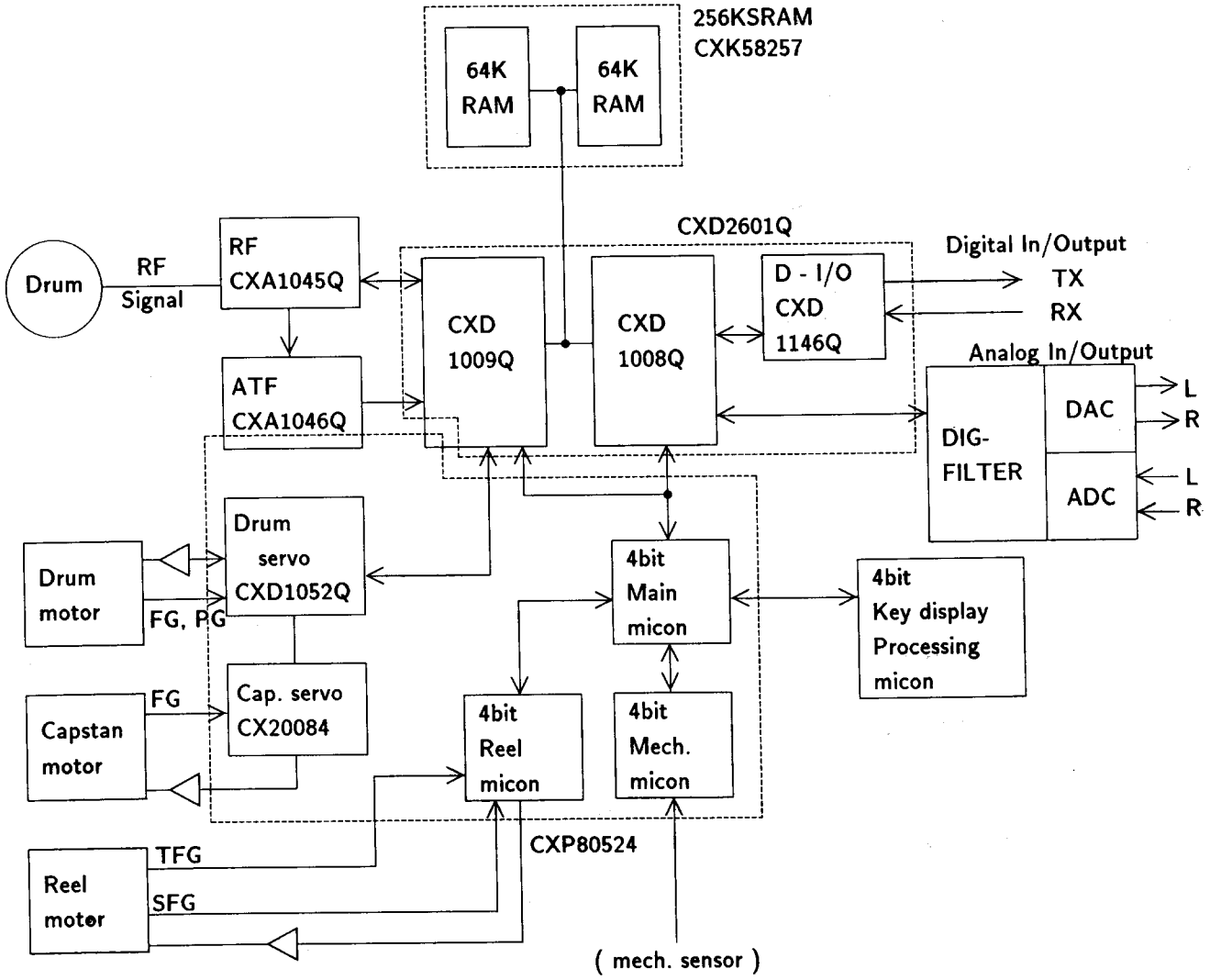


Fig. 2-1

The former signal system consisted of three chips : CXD1008 (ECC), CXD1009 (RAM control) and CXD1146 (digital I/O). The DTC-55ES, however, combines these three into the second-generation LSI chip CXD2601Q. Previously two 64-kbit RAM's were used as supplementary RAM memory ; in the DTC-55ES, a 256-kbit RAM is applied in order to margin up the data I/O timing and the NT (non-tracking) demodulation processing.

A/D conversion is achieved by 64 times oversampling the Delta-Sigma modulation (1-bit ADC) through a built-in digital filter whereas D/A converter has a built-in three-demensions noise shaper and a pulse D/A converter employing PLM system in the pulse converter.

The servo system control circuit used to include three MICON's (main/mech/reel MICON), a drum servo LSI IC (CXD1502) and a capstan servo LSI IC (CX20084). All these are now combined into one signal chip. Moreover, software servo is added to the servo circuit.

3. CXD2601 (SIGNAL PROCESSING)

The new CXD2601 combines the signal processing functions formerly performed by three different chips, viz. CXD1008 (EEC), CXD1009 (8-10 modulation) and CXD1146 (digital I/O), into one chip the features and reliability of which prove more powerful.

The CXD2601 handles all the digital signal processing operations required by the R-DAT system, as listed below :

* 8-10 modulation for the record/playback signal
* RAM control
* Error-shooting, parity production
* MICON interface (clock synchronizing system serial I/O)
* Digital PLL
* A-D/D-A control
* Generation of Fs system clocks (Fs 512Fs) and timing signal.

Main features

1) Compatibility with all R-DAT modes

   Compatibility with Fs = 48k, 44.1k, 32k, LP mode, and 15ϕ, 30ϕ DRUM is ensured.

   The new LSI enabled this as well as the LP mode (Fs = 32kHz, 12bit non-linear quantization). With the previously used LSI this was totally impossible. Moreover, 4-hour recording/playback is now possible with a 120-minute tape.

2) Compatibility with SCMS for digital I/O and high-efficiency D-PLL.

   By adopting digital PLL for RF, all the added and adjustment parts of the former analog PLL are replaced, and the PLL lock range is widened whereas the high-speed search function has become more reliable. It was investigated to which extent the relative tape/head velocity could deviate from the standard value without losing vital information.

3) Super error-correction power by new double sign

   This is achieved by using a Faust decoder, i.e. a four-stage decoder employing the feed-forward super strategy.

   Unlike the former double-sign time system which performs C1 - C2 double signing, the new LSI system carries out a C1 - C2 - C1 - C2 quadruplex signing.

   By time-dividing the double signal is multiplied (pipeline multiply decoding) the double sign is shared between the RF (PB) and the ECC blocks. This way both blocks can repeat the C1 - C2 - C1 - C2 double sign within the limitations of the timing.

   This super error-correction system considerably reduces random errors through symbol error conversion and the 10^{-3} system.

	(FORMER LSI)	(NEW LSI)
PROBABILITY OF DISABLE CORRECTION	10^{-25}	10^{-31}
PROBABILITY OF CORRECTION ERROR	10^{-35}	10^{-45}

3-1. System Construction

3-1-1. LSI Circuit Construction

The CXD2601Q handles the digital signal processing along with a 256-k SRAM and crystals. This LSI IC contains eight different circuit blocks :

1) DPLL block : digital PLL circuit for playback RF signal
2) PB block : 10-8 demodulation of playback data and data writing to RAM
3) REC block : 8-10 modulation of recording data and recording data constitution
4) ECC block : C1/C2 parity production and C1/C2 error-detecting correction in proportion to the R-DAT error-correction format
5) SUB block : sub-code data with added microcomputer, etc., I/O and D-I/O block control
6) ADA block : production of PCM data interleave address and processing of standard timing production in internal data
7) D-I/O block : AES-EBU D-I/O formatter circuit and Fs system clock production
8) RMIF block : address modulation for added RAM access and access timing production.

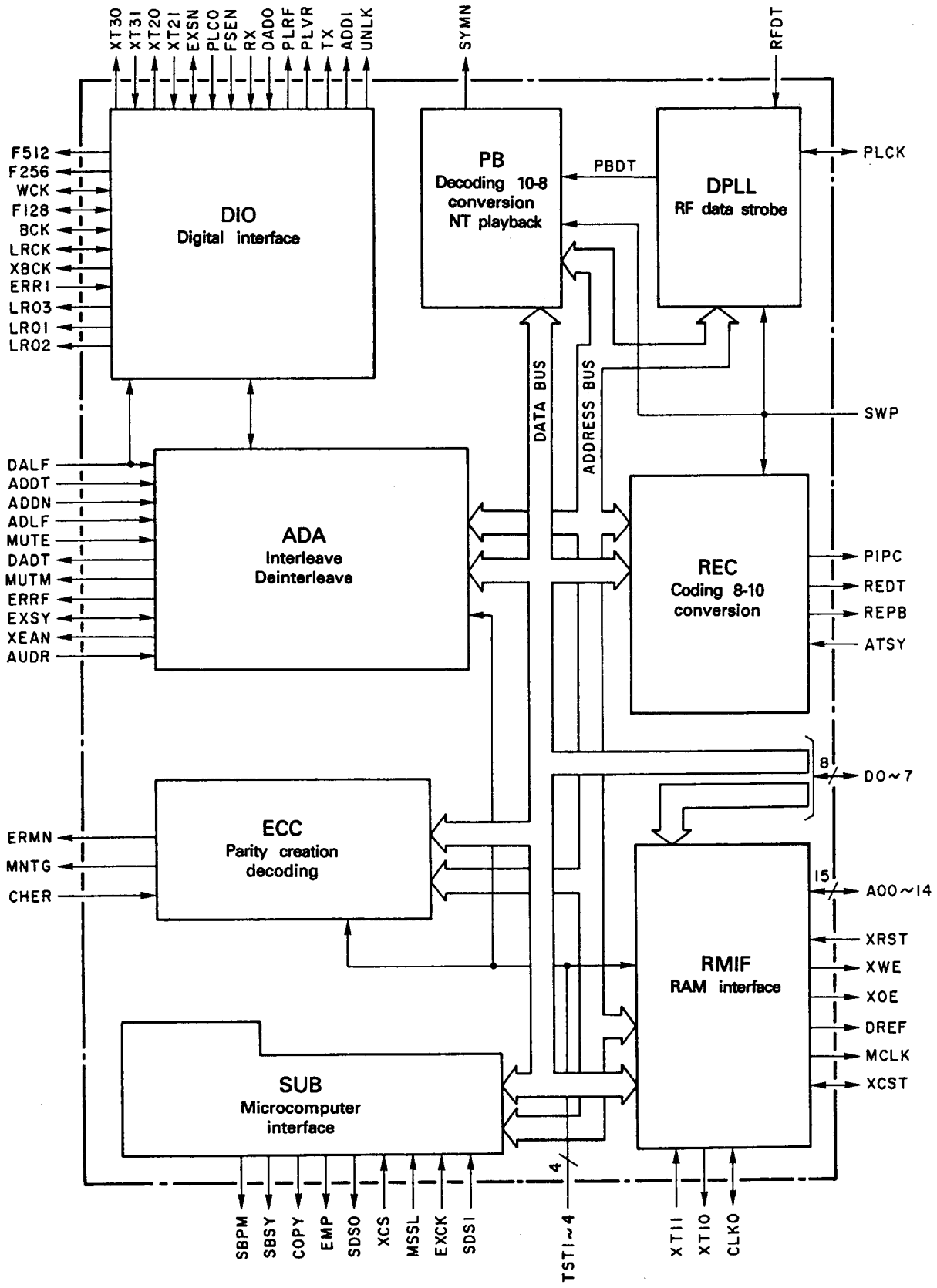


Fig. 3-1 CXD2601Q Block

3-1-2. DPLL Block

The DPLL block shown in figure 3-2 contains a period measuring part, a clock generating part, and a phase detecting part.

The period measuring part counts the clock produced inside and supplies one period to the clock generating part. In turn, the clock generating part produces clock signals at the periodic data pace.

In the phase detector, the input data is phase compared with the playback clock whereas the synchronizing signal for extracting the phase difference is supplied to the clock generator.

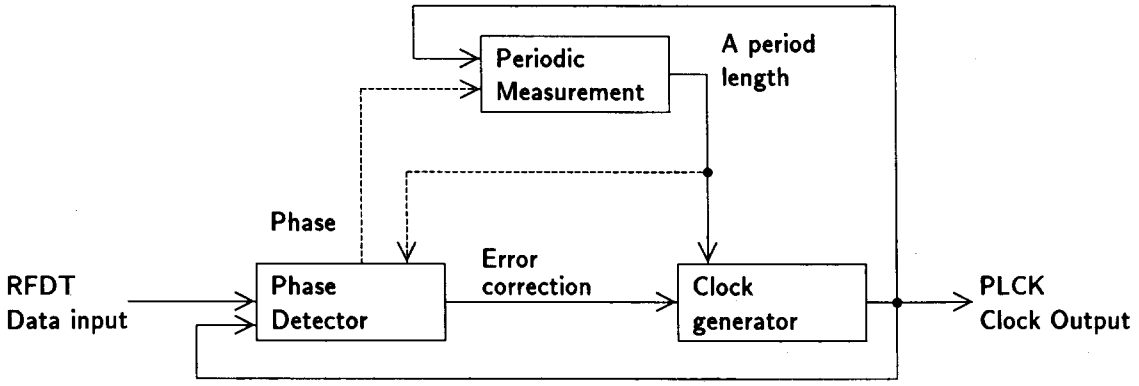


Fig. 3-2 DPLL Block

3-1-3. PB Block

The PB block handles RF signal demodulation, data writing into RAM, as well as the production of the forced interpolated signals at variable playback speed, etc.

It writes PCM data and sub-code data into the buffer RAM after demodulation.

This LSI IC carries out the so-called NT demodulation processing whenever the same track is traced mode than twice (depending on the mode). In other words, it checks the C1 syndrome of the playback data for errors ; if there is no error, the data is made ineffective when the same track (data) is read again afterwards.

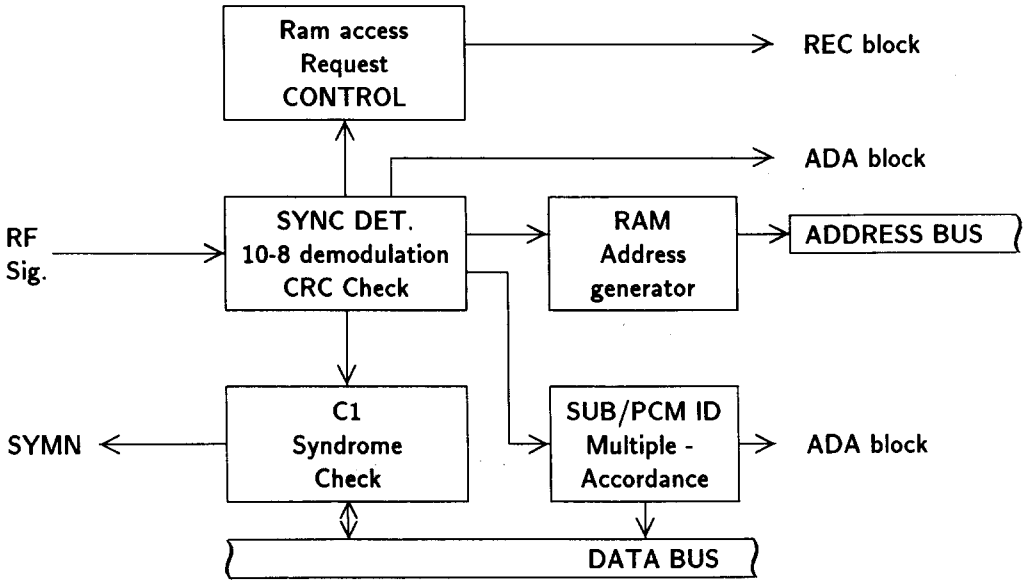


Fig. 3-3 PB Block

3-1-4. REC Block

The REC block processes the recording signal (REDT) in that it outputs both the discriminating signal (REPB) for record/playback and the discriminating signal (PIPC) for the ATF pilot signal during recording.

The record signal is output at the falling edge of the switching pulse (SWP) to the A head and to the B head record data at the rising edge.

The REC block reads the PCM and sub-code data to be recorded out of the RAM in synchronization with the timing of the standard drum signal (DREF) ; DREF and SWP need to be synchronized during recording. The timing diagram is shown in figure 3-4. It shows that the falling edges respectively the rising edges of DREF and SWP need to be within +/- 11 blocks.

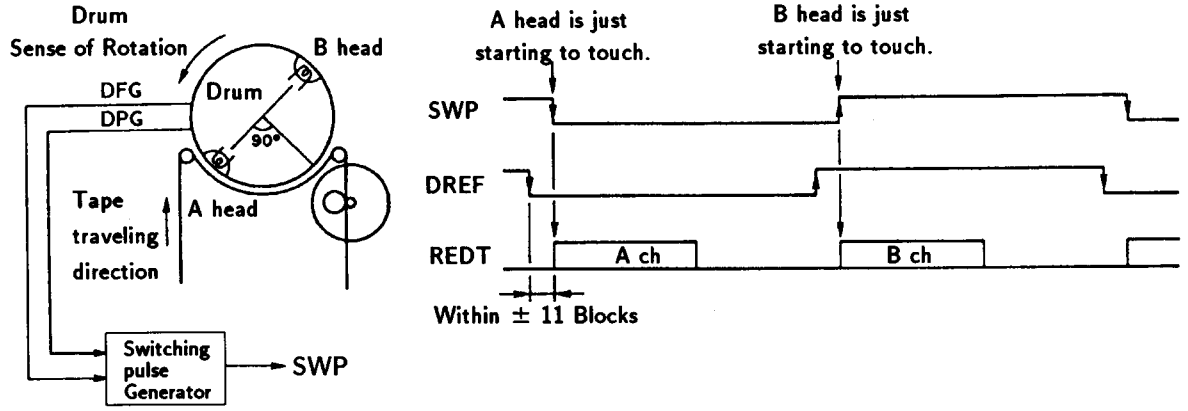


Fig. 3-4 Drum Rotation Phase Timing

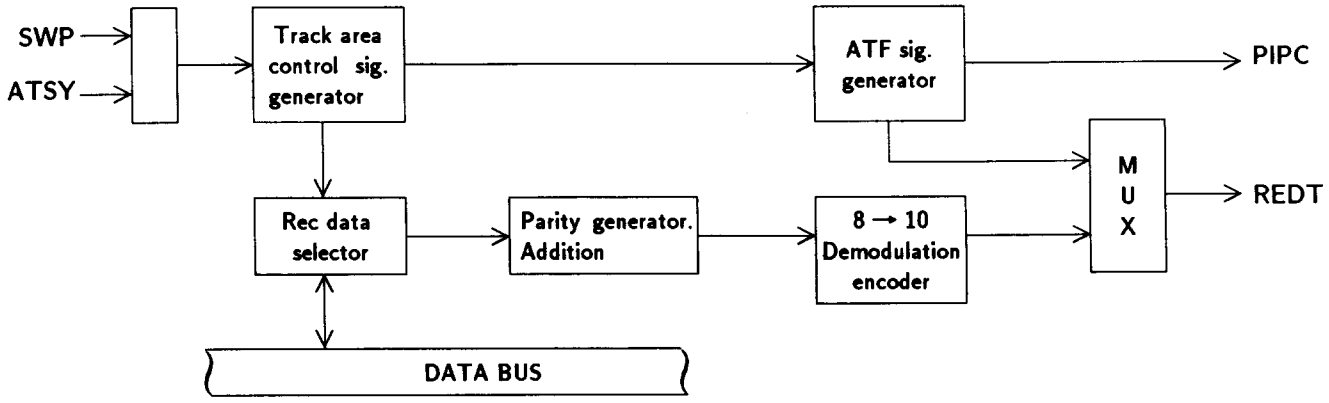


Fig. 3-5 Rec Block

3-1-5. ECC Block

In principle, the ECC block generates the C1/C2 parity during encoding and the data error-correction during decoding.

DAT ECC is a completed block-type code which is capable of double-sign repeating. By doing so, it inhibits random errors.

Formerly, double-signing used to be limited to C1 - C2 due to the length of the interleave block and the processing speed. The new LSI technique, however, divides the double-signing opration over the RF (PB) block and the ECC block. By double-signing the identified data individually, double-signing C1 - C2 - C1 - C2 is repeated within the restrictions set by the same timing in succession.

Figure 3-6 illustrates the concept of double-signing during decoding.

THE FOLLOWINGS ILLUSTRATE THE CONCEPT OF DOUBLE SIGN METHOD AT DECODING

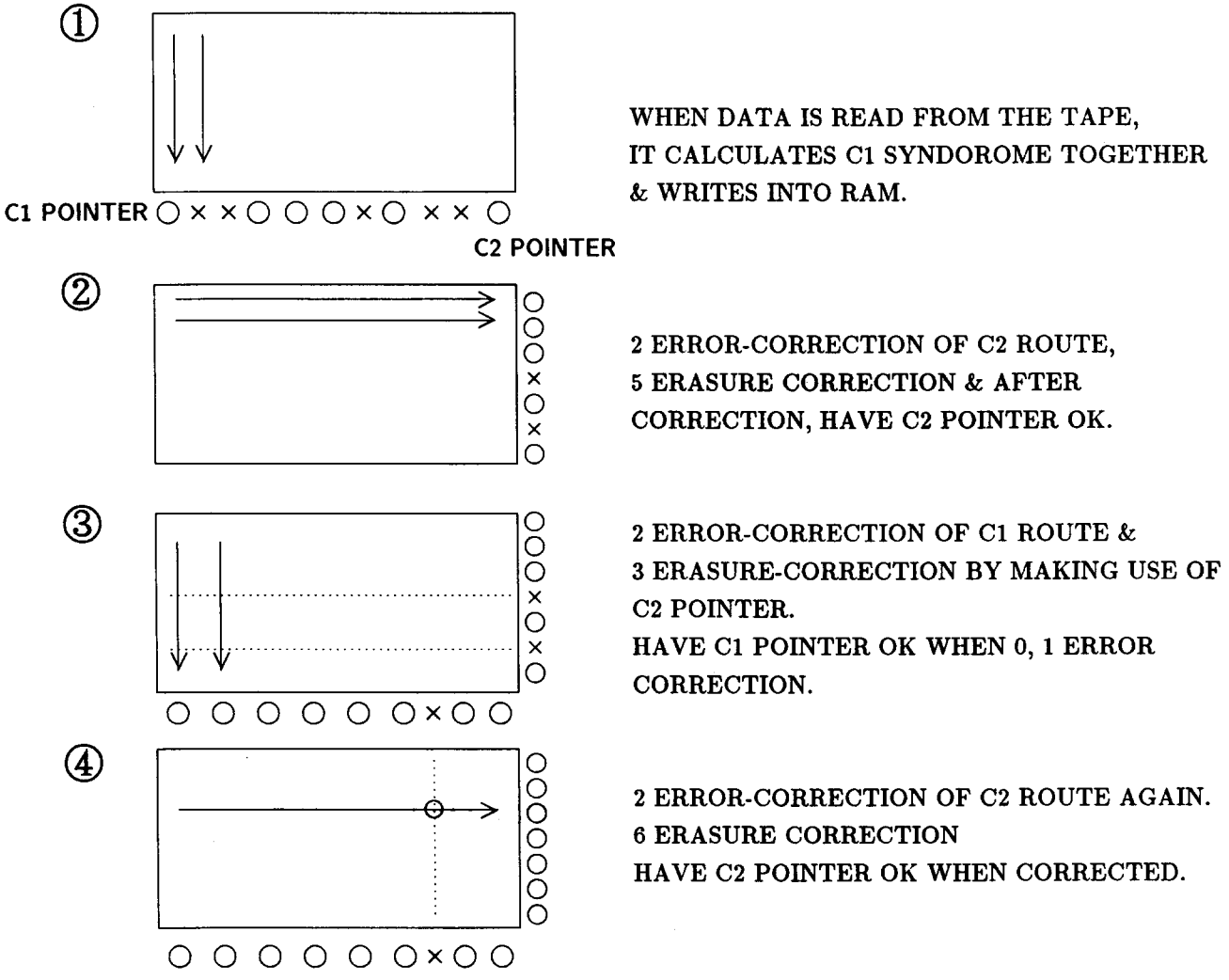


Fig. 3-6

3-1-6. Sub Block

The sub block controls inputs and output as the C bit of the sub-code data and the digital audio interface as well as the DIO block by means of an external MICON.

The interface with the MICON is shown in figure 3-7. Note that XCS and SBPM are not necessarily connected to the MICON.

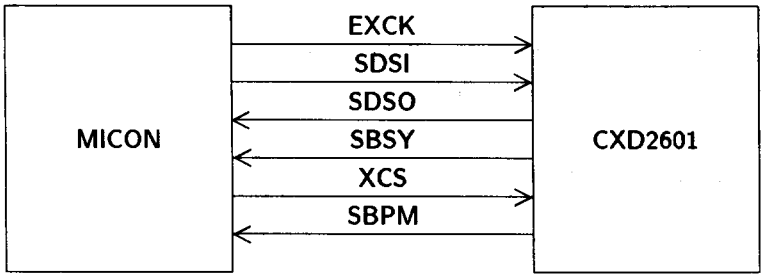


Fig. 3-7 Connection with Micon

SBSY must achieve serial I/O for 30 ms during SP and for 60 ms during LP and MICON while it is 'L'.

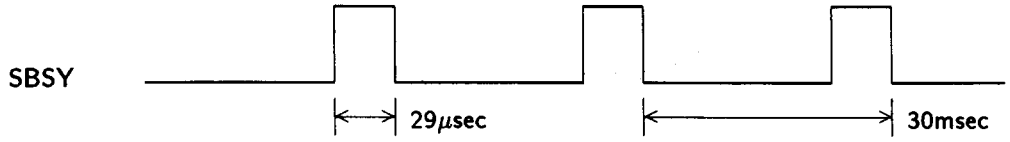


Fig. 3-8 SBSY Timing (SP mode)

Figure 3-9 shows the phase relationship between EXCK, SDSI AND SDSO.

As shown, the data changes with the falling edge of EXCK. When data is taken in, latches with the rising edge of EXCK.

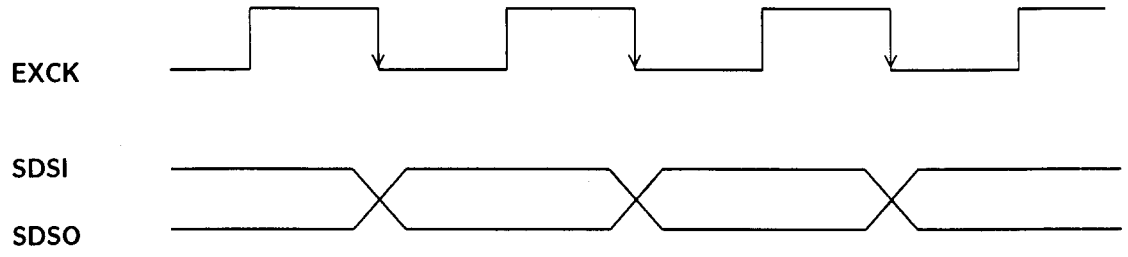


Fig. 3-9 Phase Relation between ECXK, SDSI and SDSO

3-1-7. ADA Block

The ADA block includes the PCM interleave address generation block, the A-D/D-A converter, and the interface block.

The PCM interleave address generation block produces all the interleave addresses for the SP/LP mode.

The A-D/D-A converter block and the interface block generate the interface timing, interpolation, 12 - 16 compression/expansion, as well as the waveform processing at variable speed.

If the PCM data is judged to be erroneous, it will be interpolated and output from the DADT.

The term interpolation covers both predistortion and mean value.

In the LP mode the recorded audio data word is compressed, but the input word is 12 bit instead of 16 bit. In order to restore it back to 16 bit, the audio data word from DADT and ADDT on the interface with the A-D/D-A converter is expanded by the 12 - 16 compression/expansion stage.

Figure 3-10 shows the construction of the data word and data symbol in the SP and LP modes.

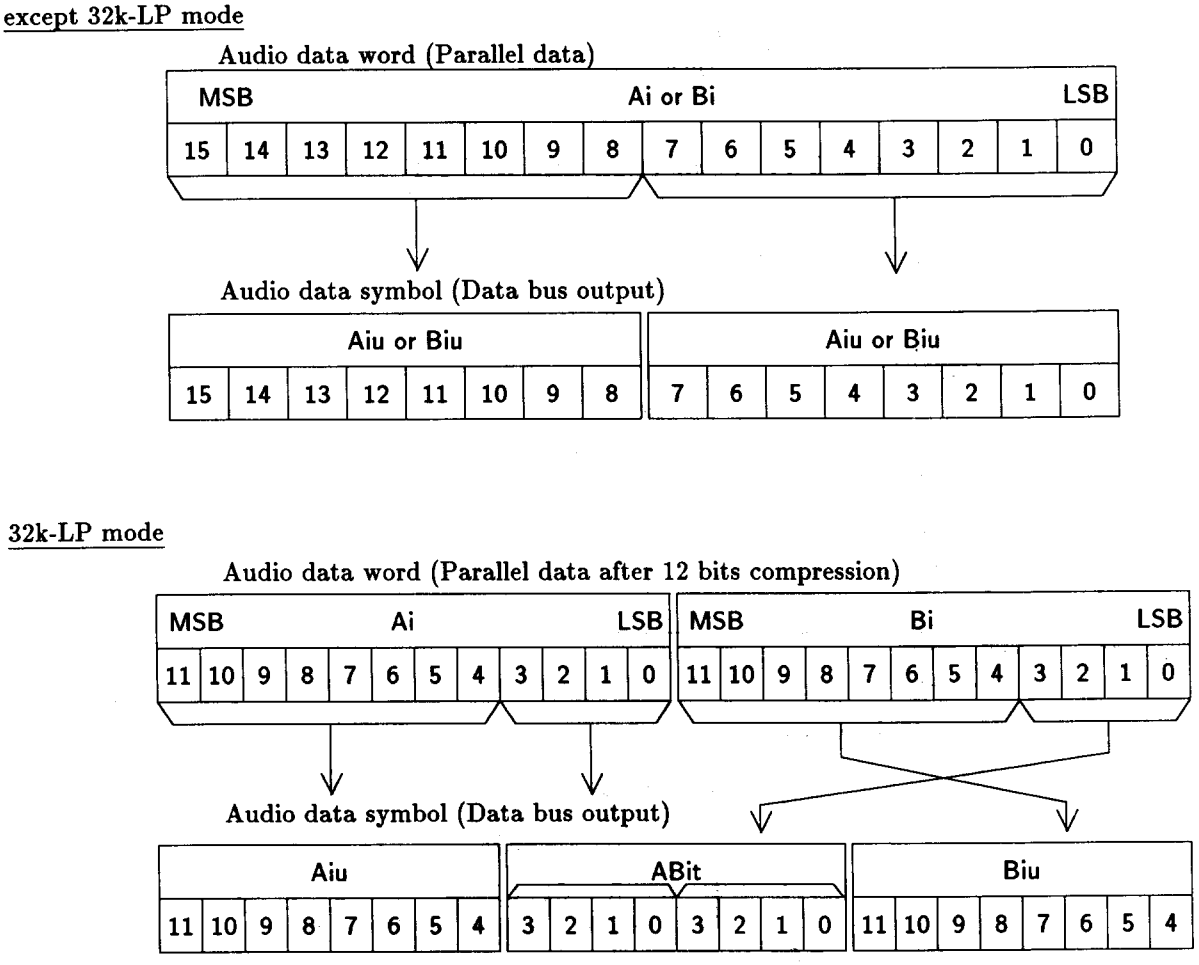


Fig. 3-10 Data Construction

3-1-8. DIO Block

Basically the DIO block performs the same functions as the CXD1146.

It handles data modulation sending and demodulation receiving for the audio interface format. Moreover, it controls the analog clock generation of the Fs system as well as the reception of the demodulation clock extracted from the PLL circuit.

Figure 3-11 shows that DIO block is connected to the MICON via a sub-I/O block for control. The DIOO and DI01 lines are used for sending PLL lock condition channel status information amongst others.

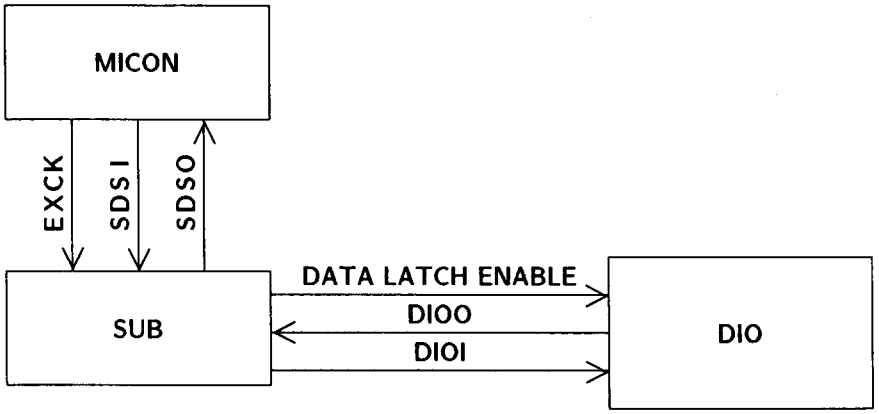


Fig. 3-11 Connection with MICON

Figure 3-12 shows an example of an analog PLL circuit.

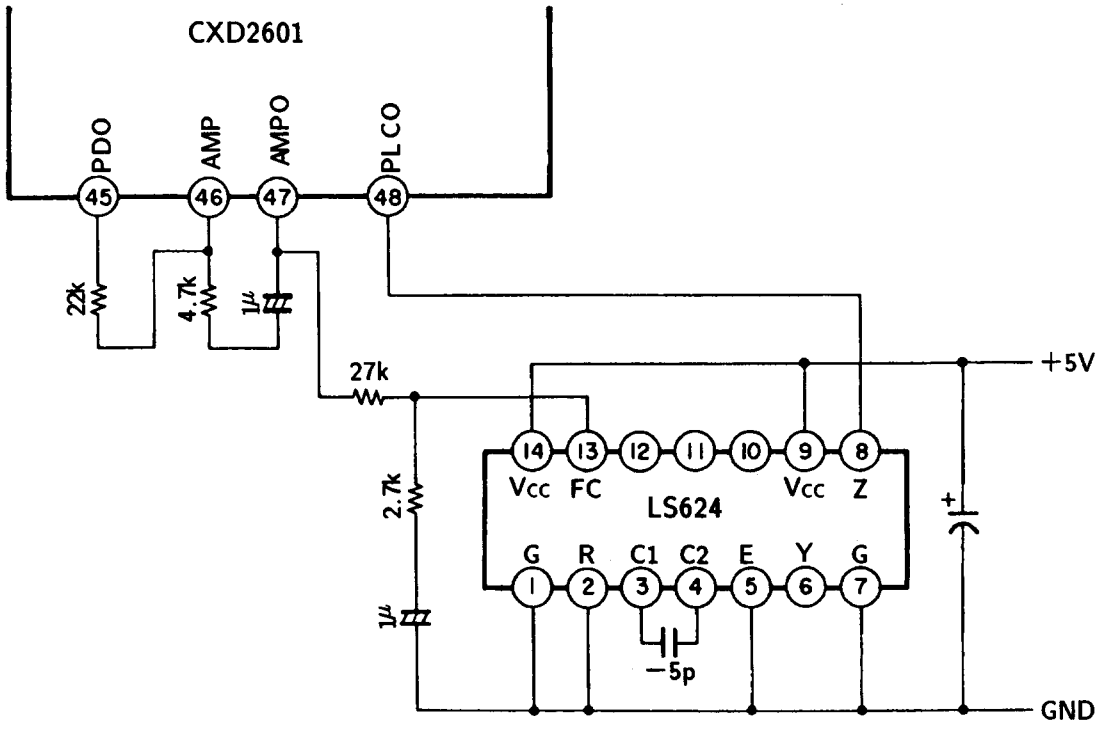


Figure 3-12. Analog PLL circuit

3-1-9. RMIF Block

The RMIF block serves to produce the RAM I/F signal (ADDRESS/OE/WE), to control the RAM access request from each block, and to generate the SYCK/MCLK/DREF pulses. SYCK is the system clock stage which carries out all access operations.

Normally the 4.704MHz frequency with 50% duty is frequency-divided from the 18.816 MHz CLKO pulse. The DTC-55ES is connected internally by the 18.816 MHz frequency of XT11/XT10 and CLKO.

The 9.408 MHz MCLK pulse is generated by halving the CLKO for the drum servo reference signal.

The DREF (drum servo reference signal) is the signal derived from the interleave reference on which the SYCK clock is superimposed. It is 50/3 Hz in the LP mode and 100/3 Hz in the SP mode. On the contrary, the search mode is installed by frequency-dividing the PLCK pulse (clock extracted by RF DPLL).

4. CXP80524 (SYSTEM CONTROL, SOFTWARE SERVO)

The CXP80524 controls the R-DAT mechanism, servo control and built-in peripheral hardware for facilitating the sub-code processing. It is a microcomputer capable of performing the highly efficient R-DAT control with fewer added circuitry.

The advantage of this MICON is that it unites all the functions performed by the CXD1052 (MAIN/MECHANISM/REEL and DRUM SERVO), the CX20084 (CAPSTAN SERVO), and part of the CXA1046 (AFT). Its main features are described below.

1) 24-kbyte ROM (with built-in 576-byte RAM)
   Master clock : 9.408 MHz (supplied by CXD2601)
   Processing speed : 425 ns
2) Built-in 8-bit A/D converter
   After 8 bit A/D conversion the analog 130-kHz ATF pilot signal is fed to the CXP80524 where it is treated as a digital signal. Thanks to this, the temperature characteristics towards all added parts need not be taken into consideration. Moreover, the speed adjusting VR is no longer required.
   This extensively improves the reliability during playback.
3) Serial interface with buffer RAM
   A serial interface of the clock-synchronizing type with 96-byte RAM is built in.
4) Drum FG/PG, capstan FG, reel FG input circuits with built-in PWM output circuits
   Thanks to the software servo used for the drum/capstan servo and the reel servo during high-speed search, no speed adjusting VR is required.
   This all-digital servo system is extremely stable and not liable to temperature or variations of any other kind.

4-1. Peripheral Hardware Overview (CXP80524)

Block Name		Functions/Features
Calculation Coprocessor		Increases processing power by performing calculations in parallel within the CPU. Calculation functions provided include 16-bit x 16-bit multiplication, 32-bit/16bit division; 24-bit multiply-and-accumulate, and multiple bit shifts and rotations.
ATF Sync Detector		Detects ATF sync signals in playback data (RFDT), from the rotating head, and generates sampling pulses for tracking. The sampling pulses are input to the A/D converter unit for A/D conversion timing, allowing for automatic conversion.
A/D Converter Unit		A sample-hold A/D converter with 8 channels of analog input and 8-bit resolution. Since a function for realtime control of conversion start timing is provided, analog voltages can be measured with precise timing.
Serial Interface Unit		A clock synchronized serial interface. It includes a 96-byte on-chip buffer RAM and a chip-select automatic transfer mode.
Timer/Counter		Configured with two independent 8-bit T0 and T1. They can be used as two interval timers, or T0 can be used as an event counter. If T0 and T1 are cascaded, they become a 16-bit timer/counter.
Prescaler/Time-Base Timer		The prescaler divides the oscillation clock and supplies this divided clock to peripheral hardware. The time-base timer (TBT) generates reference time interrupts of a watchdog function.
Servo Input Control	Capstan Input	An input control circuit for capstan servos. The capstan FG input Pulses can be frequency divided with a 6-bit programmable frequency divider. To help prevent motor runaway, a capstan mask timer that prohibits the generation of regularly space interrupts is provided on-chip.
	Reel Input	An input control circuit for reel FG measurement. Reel FG input pulses can be frequency divided with a 6-bit programmable frequency divider.
	Drum Input	An input control circuit for drum servos. Drum PG inputs and drum FG inputs are provided. The frequency division ratio of drum FG input pulses can be selected from 1/1, 1/2, 1/4, 1/8, or 1/16.
SWP Signal Generator		Generates a signal (SWP) synchronized to the drum rotation rate based on the drum FG or the drum PG. A 4-bit programmable frequency divider and a 14-bit timer for SWP signal generation are provided on-chip, allowing variable SWP delay lengths.
PWM Generator		Includes 12-bit PWM output (2 pins) and 8-bit PWM output (3pins). The outputs are converted to analog voltages by passing them through an external low-pass filter.
FRC Capture Unit		Configured around a high-speed 22-bit up-counter (FRC). The FRC value is latched based on the timing of edge detection of input pulses. This allows the phase error between pulse periods (motor rotation velocity detection) and a reference signal measured with high accuracy. In particular, measurement precision for drum motor rotational velocity detection is 212 ns (when oscillation is 9.408 MHz).
Programmable Pattern Generator		Can generate 11 high-precision realtime pattern output simultaneously. The timing precision is 850 ns (when oscillation is 9.408 MHz), so it can be used for applications requiring accuracy with many types of timing outputs.

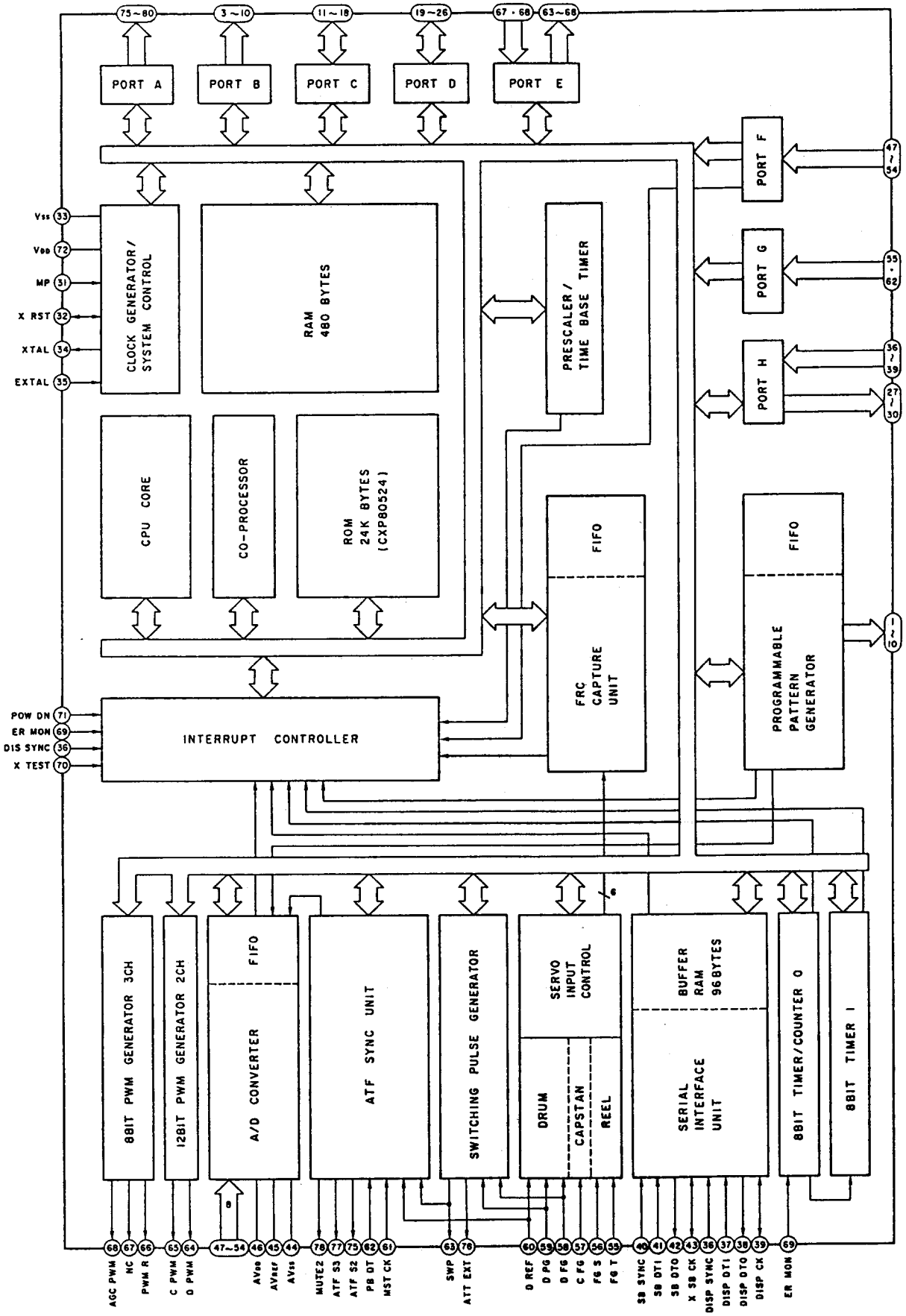


Fig 4-1. BLOCK DIAGRAM

4-2. Software Servo

The software servo accurately measures the on-time between successive FG edges through the MICON peripheral shown in figure 4-2.
The FRC is a free-run counter fulfilling a clock function, i.e. the edge timing is recorded by latching the FRC data by the edge detecting signal.
This method of calculating the FG period gives the same information as eventual angle speed information.

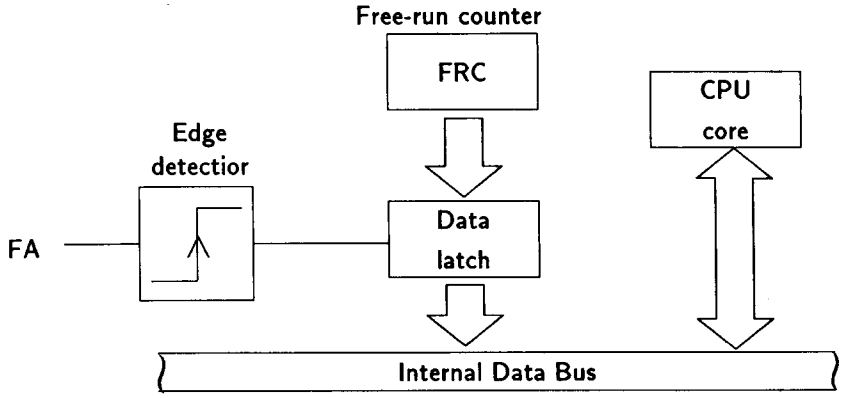


Figure 4-2. REAL TIME INPUT PREFERAL

Figure 4-3 shows how the FG period row t1, t2, t3, is calculated upon receiving the edge detecting row t1, t2, t3, ...

$$Tn = tn+1 - tn$$

Whereas Angle SPEED ERROR En :

$$En = \frac{2\pi}{tn+1 - tn} - \frac{2\pi}{T_{REF}}$$

IF $T \approx T_{REF}$:

$$En \fallingdotseq \frac{2\pi}{T_{REF}^{\,2}} (tn+1 - tn - T_{REF})$$

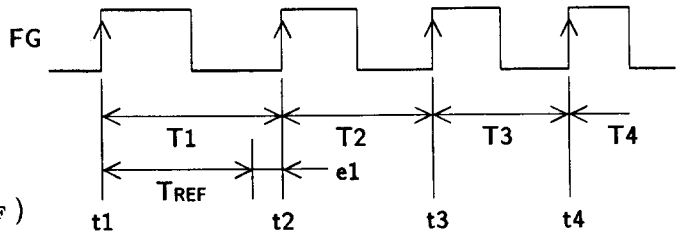


Figure 4-3. TIME ROW & SPEED ERROR

The software servo system calculates the angle speed error by comparing the timing of the edge detecting signal of the FG pulse with a preset reference value. The resulting PWM output waveform from CXP80524 then passes through s low-pass filter to convert it into an analog voltage before being fed to the motor drive circuit and the motor itself (see figure 4-4).

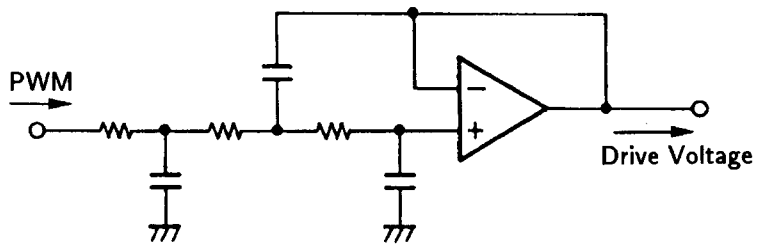


Figure 4-4. Low-pass filter to eliminate carrier frequency component from PWM

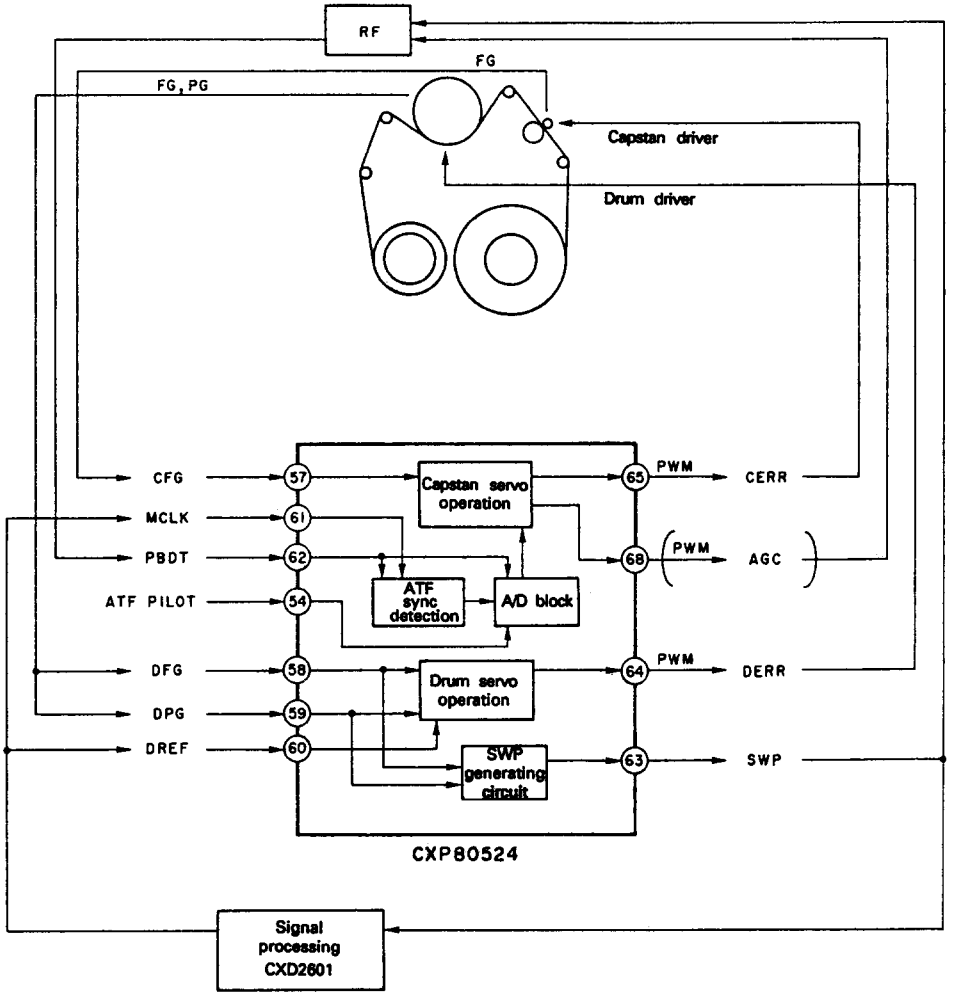


Figure 4-5. Capstan/ drum servo system

Figure 4-6 shows the priciple of the capstan software servo block.

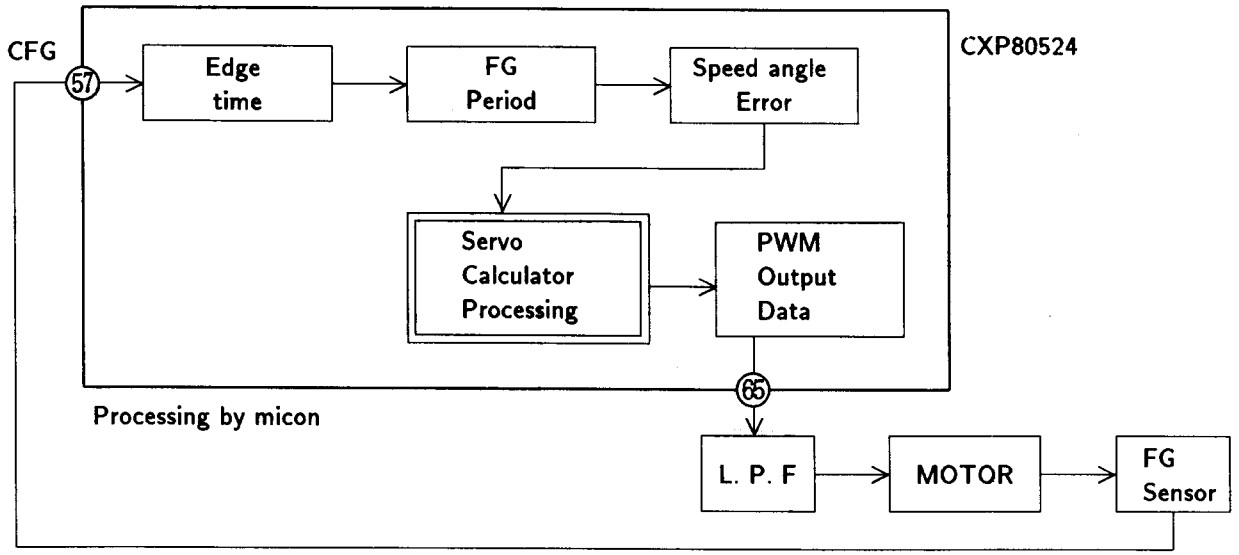


Figure 4-6. Capstan software servo block

In the drum servo system the DREF (drum reference) pulse with standard PG and phase is added up to control the phase angle. Its principle is shown in figure 4-7.

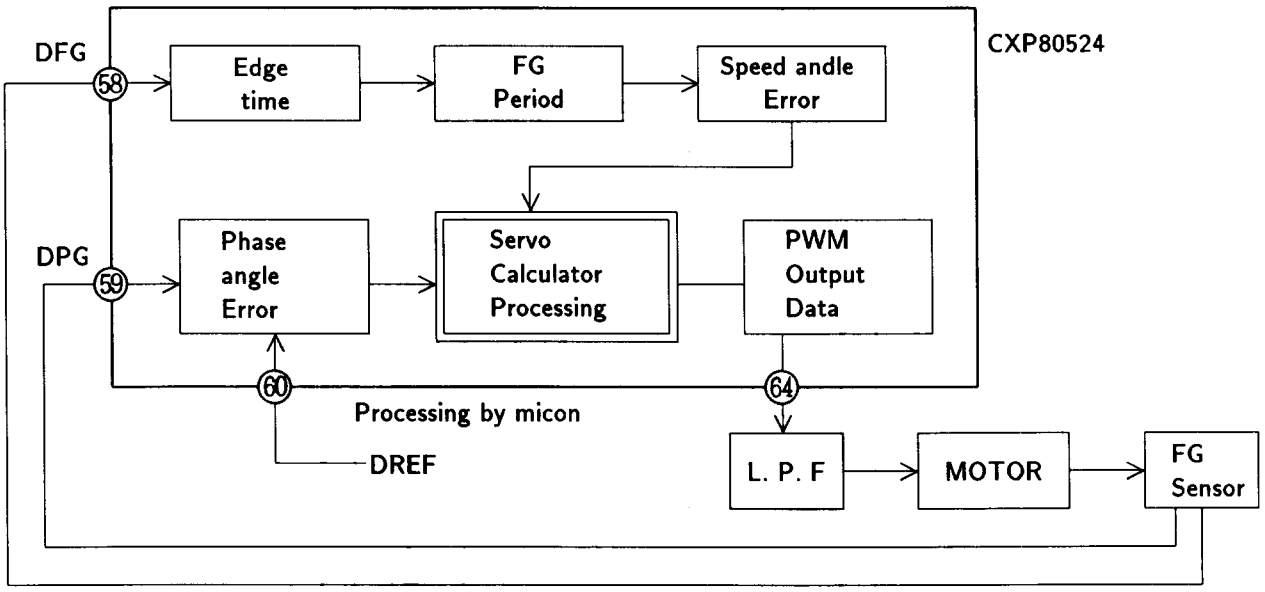


Figure 4-7. Drum software servo block

4-3. Capstan and Reel Input Control

The capstan and reel input control circuit performs capstan/reel motor velocity and phase error detection for servo control. As shown in figure 4-8 the circuit is configured with a capstan FG input unit and a reel FG input unit.

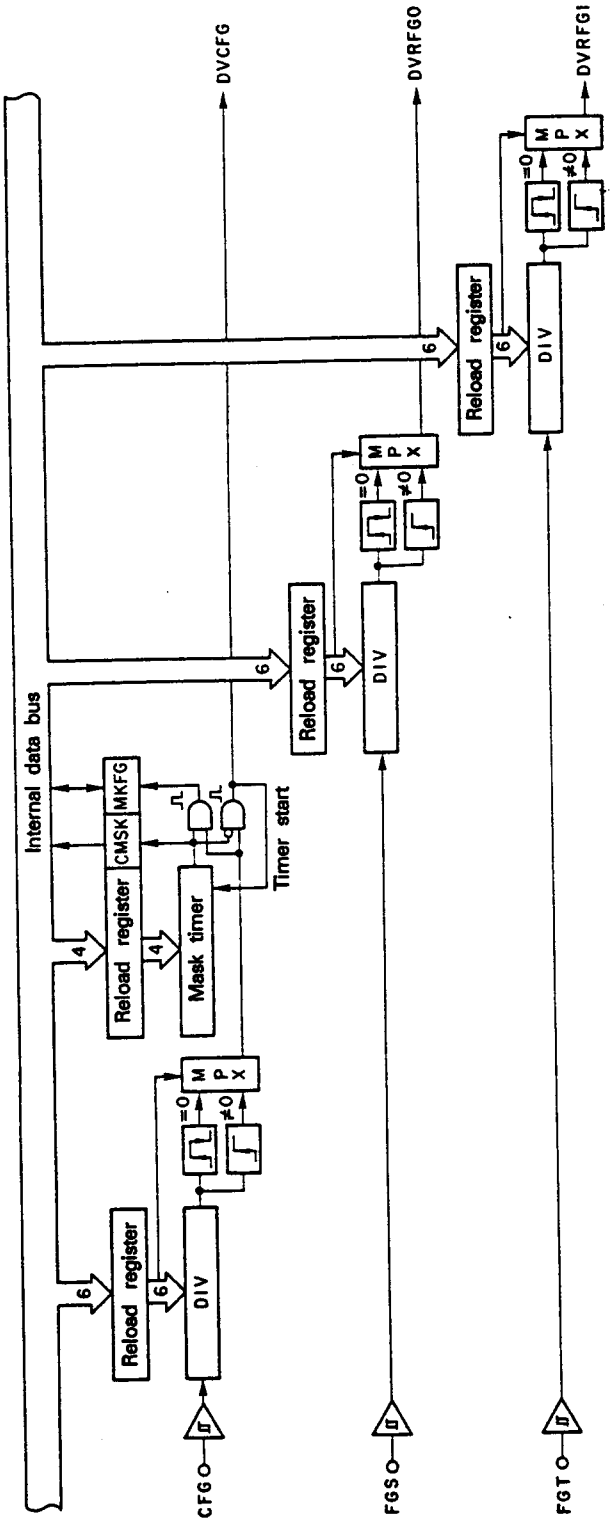


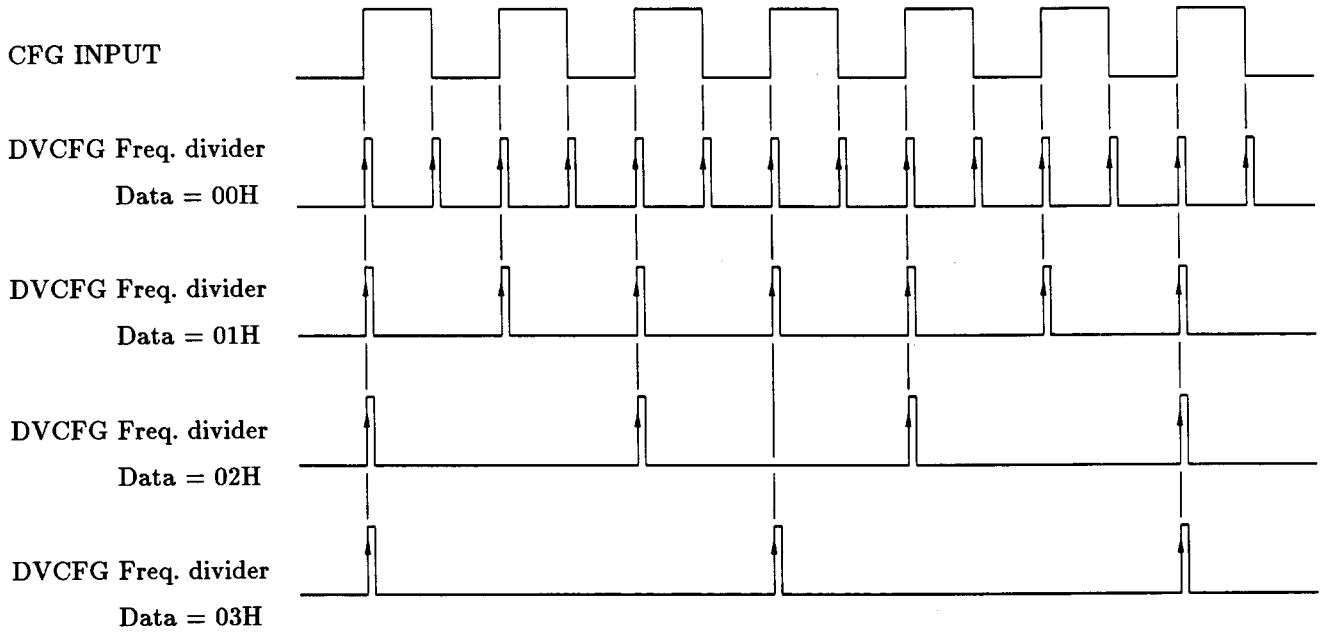
Figure 4-8. Capstan and reel FG input cotrol block

4-3-1. Capstan FG Input Unit

The FG (frequency generator) pulse output from the capstan motor is amplified and wave-shaped and then input to the CFG input pin.

The input signal passes through a Schmitt circuit and is then divided with a 6-bit programmable frequency divider.

When either the rising edge or both edges of the divided signal are detected, the signal will be sent to the FRC capture unit as the DVCFG signal after the capstan mask-time elapses.



DVCFG↑ in fig. shows the timing of edge detector at FRC capture unit.

Fig 4-9. Edge Detector Signal DVCFG

4-3-2. Capstan Mask Timer (CAPMT)

Because the rotational velocity of a capstan motor can vary over a wide range, abnormal rotation (runaway) can occur. The capstan mask timer masks edge detection at fixed intervals such that extraneous edge detection caused by abnormal rotation does not occur. The capstan mask timer starts timing after an edge detection of the frequency-divided capstan FG. While masking is in progress, all edge detection signals are masked. (Refer to Figures 4-10 and 4-11)

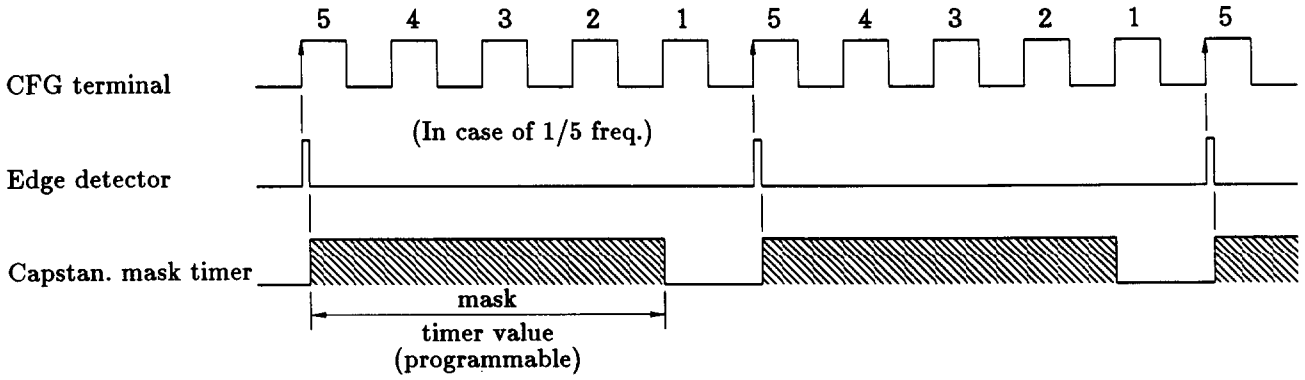


Fig 4-10. Capstan Mask Timer Operation Timing (CFG normal)

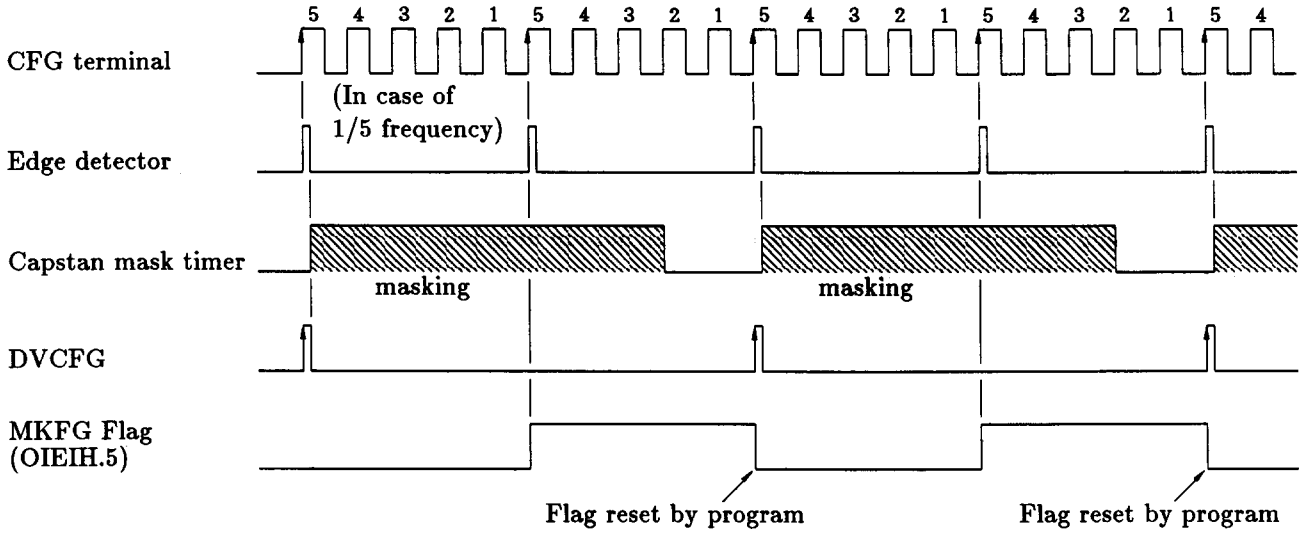


Fig 4-11. Capstan Mask Timer Operation Timing (CFG runaway)

4-3-3. Reel FG Input Unit

The FG pulse output from the reel unit is amplified and wave-shaped, and then input to the RFG0 and RFG1 input pins. (Fig. 4-8)

The input signals pass through a Schmitt circuit and are then frequency divided with a 6-bit programmable frequency divider. When either the rising edge or both edges of the divided signal are detected, the signal will be sent to the FRC capture unit as the DVRFG0 and DVRFG1 signals.

The 6-bit programmable frequency divider is configured as a reload register and a down counter. Operation is completely identical to the capstan FG input unit.

4-4. Drum Input Control and SWP Signal Generation Circuit

Analog with performing the drum motor velocity/phase error detection necessary for servo control, this circuit generates an SWP signal that indicates the number of drum rotations. As shown in Figure 4-12, it is configured with a drum FG/PG input unit and SWP signal generation unit.

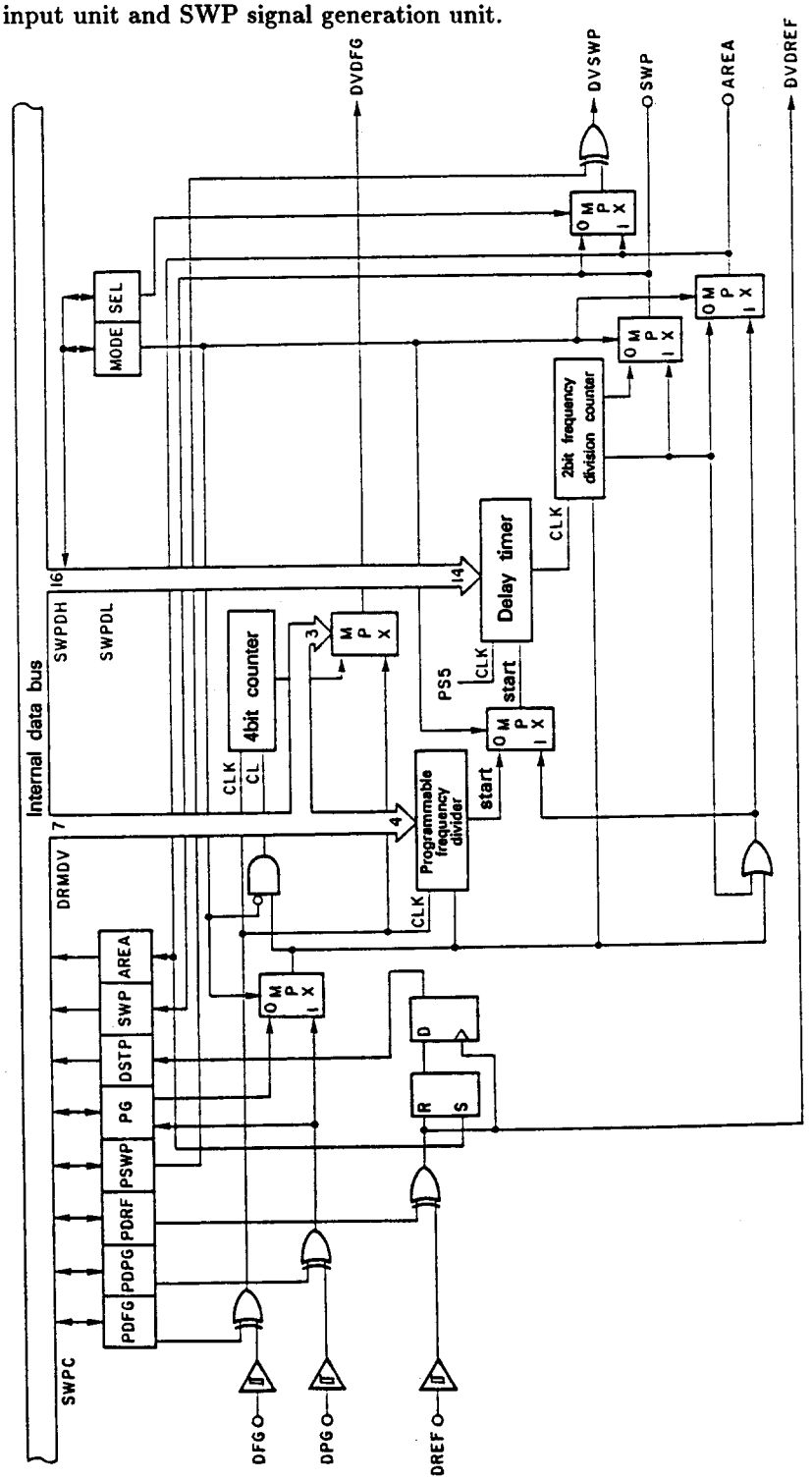


Figure 4-12. Drum input control and SWP signal generation circuit

4-4-1. Drum FG/PG Input Unit

The FG and PG (pulse generator) pulses output from the drum motor are amplified and wave-shaped and then input to the DFG and DPG input pins.

The input signals pass through a Schmitt circuit and then can be passed through or inverted depending on the polarity control of the SWP Control Register (SWPC : address 01E3H) bits 7 and 6. DFG can then also be passed through or frequency divided by 1/2, 1/4, 1/8, or 1/16, depending on the lower three bits of the Drum Input Control Register (DRMDV : address 01E2H). This signal is then sent to the FRC capture unit as the DVDFG signal.

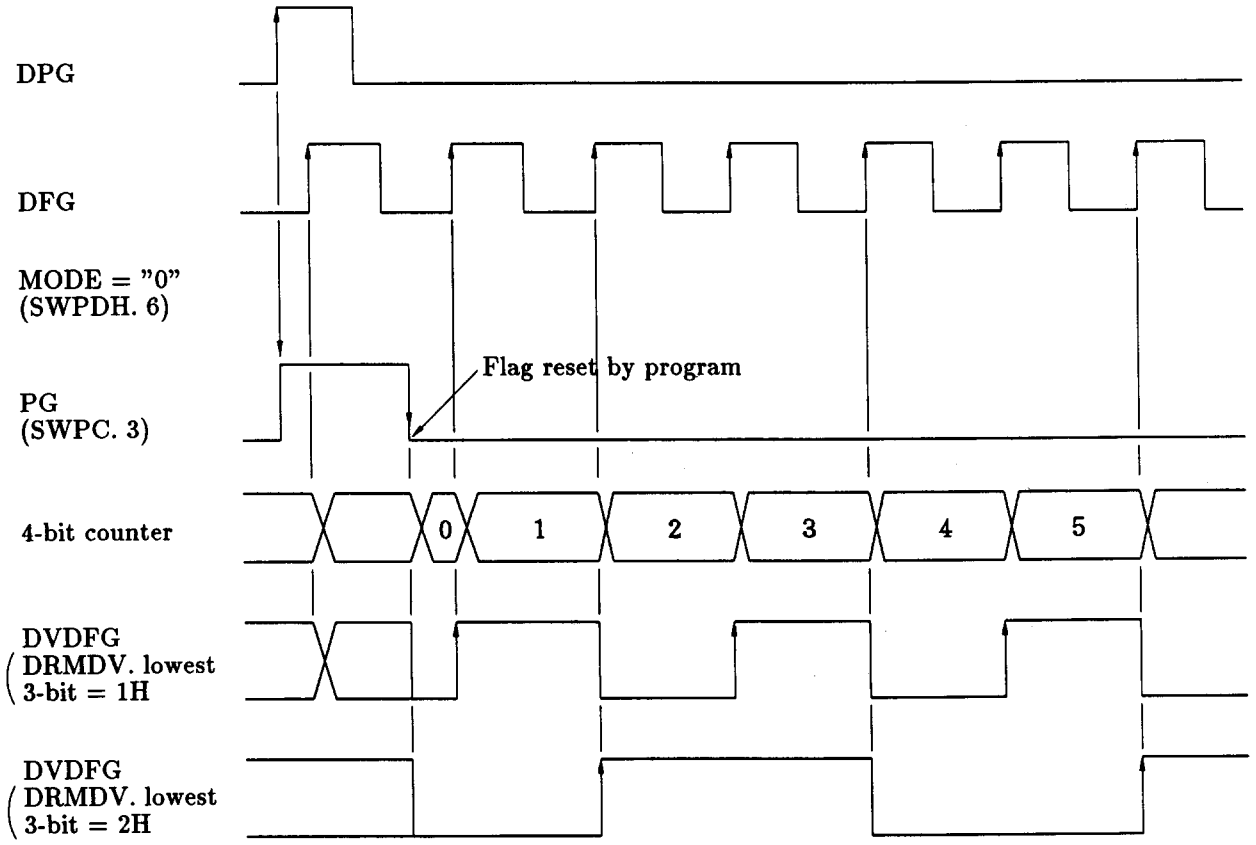


Fig 4-13. DFG Frequency Timing

As shown in Figure 4-13, when MODE = "0", the 4-bit counter is cleared by the SWP Control Register (SWPC : address 01E2H) bit 3 (PG) falling. The count operation will start with the DFG signal rising. When MODE = "1", count operation will start with the DFG signal falling, but the 4-bit counter will not be cleared. The rising edges of the DVDFG signal in the figure indicate the timing of edge detections for the FRC capture unit.

4-4-2. SWP Signal Generation Unit

The SWP signal generation unit is configured with a 4-bit programmable frequency divider, a 14-bit programmable timer, and a 2-bit frequency divider. The SWP signal can be used to indicate the number of drum rotations.

SWP Signal Generation

The SWP signal is to be generated using DPG and DFG as references.

Figure 4-14 shows the timing prior to SWP signal generation. In this mode, the SWP signal is generated using the DPG and DFG inputs, the 4-bit programmable frequency divider, the 14-bit delay timer, and the 2-bit programmable frequency divider.

To generate the SWP signal, first a falling edge must be created on the SWP control register (SWPC : address 01E3H) bit 3 (PG). This bit will be set to "1" automatically when DPG rises or when a "1" is written to it. After this bit is set, a falling edge on PG can be created by writing a "0" to it.

The 4-bit programmable frequency divider is loaded with frequency division data when PG falls and counts when DFG rises.

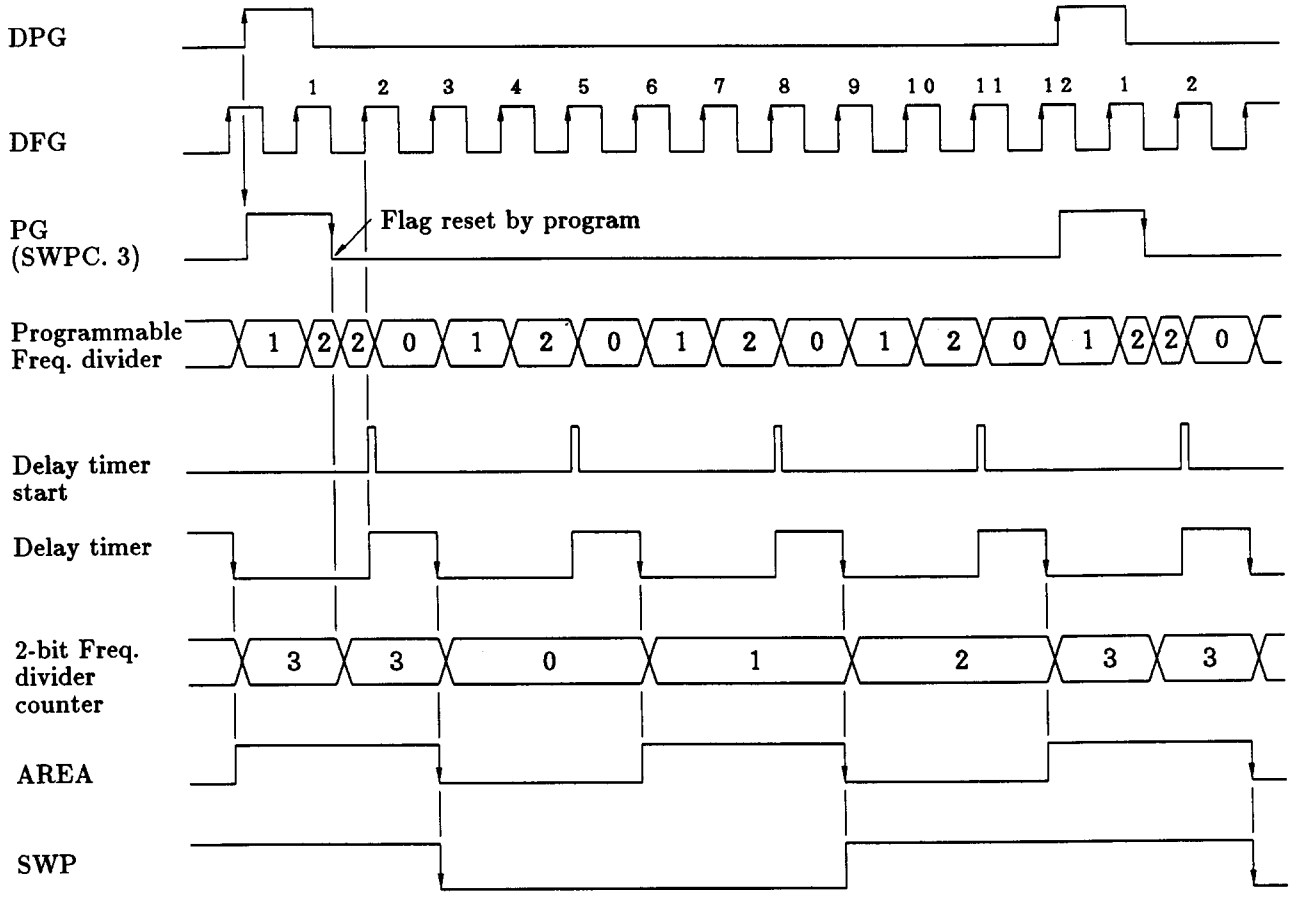


Fig 4-14. SWP Signal Generation Timing

4-5. FRC Capture Unit

The FRC capture unit can measure the timing of signal variations with high precision.

It is configured around a 22-bit FRC (free-running counter) and a FIFO. It can measure 7 external and internal signals. When the FRC capture unit detects a pulse edge, the FRC count value will be latched into the FIFO. Since a 6-level FIFO is included on-chip, inputs will be latched into the FIFO correctly even if they come immediately in succession. By subtracting the previously latched value from the currently latched value, a pulse's period can be measured.

Table 4-1. FRC Specifications

Item	Specification
FRC input clock	4.704 MHz (f_{EX} = 9.408 MHz)
FRC measurement resolution	Drum : 212ns
	Other : 850ns
Input sources (7 available)	Drum (DVDFG)
	Capstan (DVCFG)
	Drum reference (DVDREF)
	Switching pulse (DVSWP)
	Reel 0 (DVRFG0)
	Reel 1 (DVRFG1)
	Soft Trigger
Interrupts	Generated (IRQFRC)

Internal signals are DVDFG, DVCFG, DVRFG0, and DVRFG1 from the servo input control circuit (refer to Figure 4-8 and Figure 4-12) and DVSWP and DVDREF from the head amp switching signal generation circuit (refer to Figure 4-12). Also, there is a software trigger input from the program. The falling edges of DVDREF and DVSWP and the rising edges of all other signals are detected.

4-6. ATF Sync Detection Unit

The ATF sync detection circuit detects the AFT sync signal from the rotating head's playback data (RFDT) and generates ATF sampling pulses (ATFS1, ATFS2, ATFS3). For further details, refer to Section 9. (refer to Figure 4-16)

ATF sampling pulses are input as A/D conversion timing to the A/D converter unit. They can start A/D conversion automatically.
ATF sampling pulses can be output to external pins. As shown Figure 4-15, they pass through an AND circuit with PPG Control Status Register (PPGC : address 00EA$_H$) data and an OR circuit with Port A data before being output.

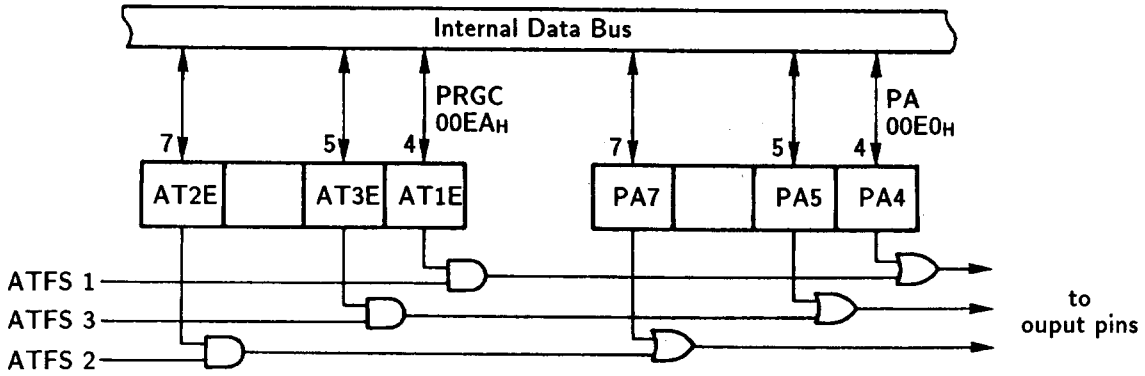
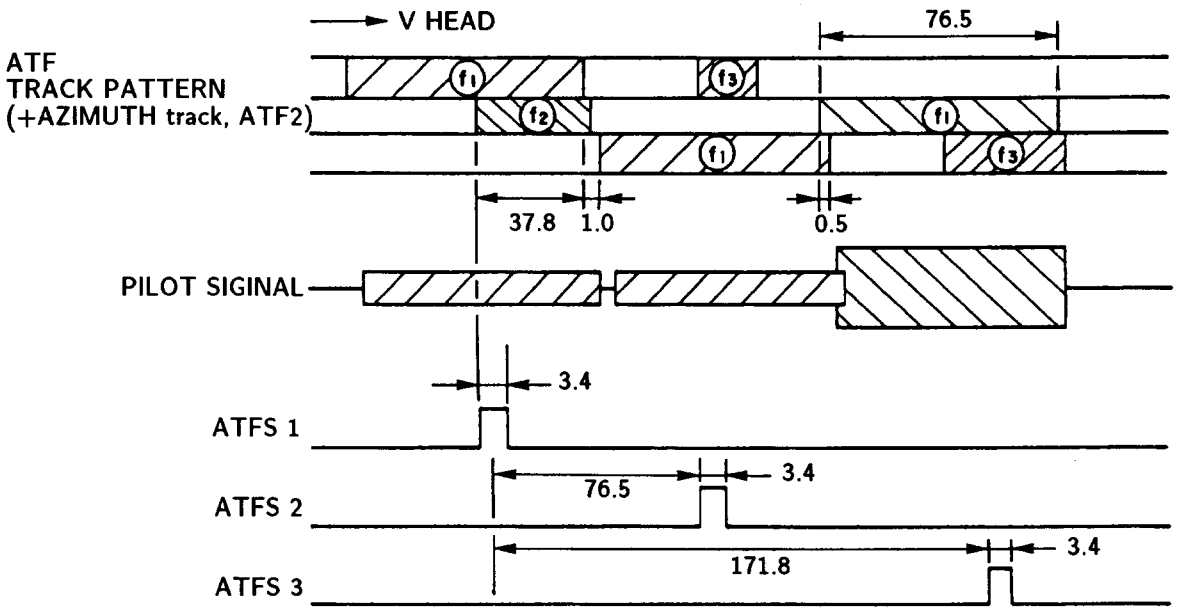


Fig 4-15. ATF Sampling Pulse Output Circuit



note) The unit of the numbers above is when the channel clock of normal playback time (μ sec) is 9.408MHz.

Fig 4-16. ATF Sampling Pulse Timing

4-7. PMW Pulse Generator

The PWM pulse generator outputs PWM-type pulses (pulse width modulation) with fixed periods and variable duty cycles. It is used to create analog voltages for applications.

There are two channels of 12-bit PWM pulse generators and three channels of 8-bit PWM pulse generators. Each can be controlled independently.

The 8-bit PWM pulse generators are configured around an 8-bit counter. They include an 8-bit data register, compare register, and comparator. As shown in Figure 4-1, the PWM outputs have a fixed pulse period but their duty can be varied by the program.

The 12-bit PWM pulse generators are configured around a 12-bit counter. They include a 12-bit data register, compare register, and comparator. As shown in Figure 4-19, the PWM outputs have a fixed pulse period but their duty can be varied by the program. The output waveform is 16 repetitions of a primary 8-bit PWM output wave. The duty is controlled by adjusting a pulse width that specifies the total width of the 16 PWM pulses. These output pulses can be turned into a DC voltage by smoothing them through an external low-pass filter circuit.

Table 4-2. PWM Pulse Generator Specifications

Item	Specification
Resolution	12 bits (2 pins), 8 bits (3 pins)
Reference clock period	106 ns (f_{EX} = 9.408MHz)
PWM iteration frequency	36.75kHz

4-7-1. PWM Output Operation

(1) 8-bit PWM pulse outputs

First the 8-bit output data must be written to one of the data registers (PWM0 - PWM2). Next, clear to "0" the bit in the Port E/SWP, PWM output selection register that corresponds to the channel to be output. By switching the port to PWM, PWM pulses will be output. The bits will be "0" after reset.

The PWM is free-running, so PWM pulses will be output continuously. The transfer of data from the data register to the compare register is performed by writing to the data register. The timing of the transfer is once per period of the counter.

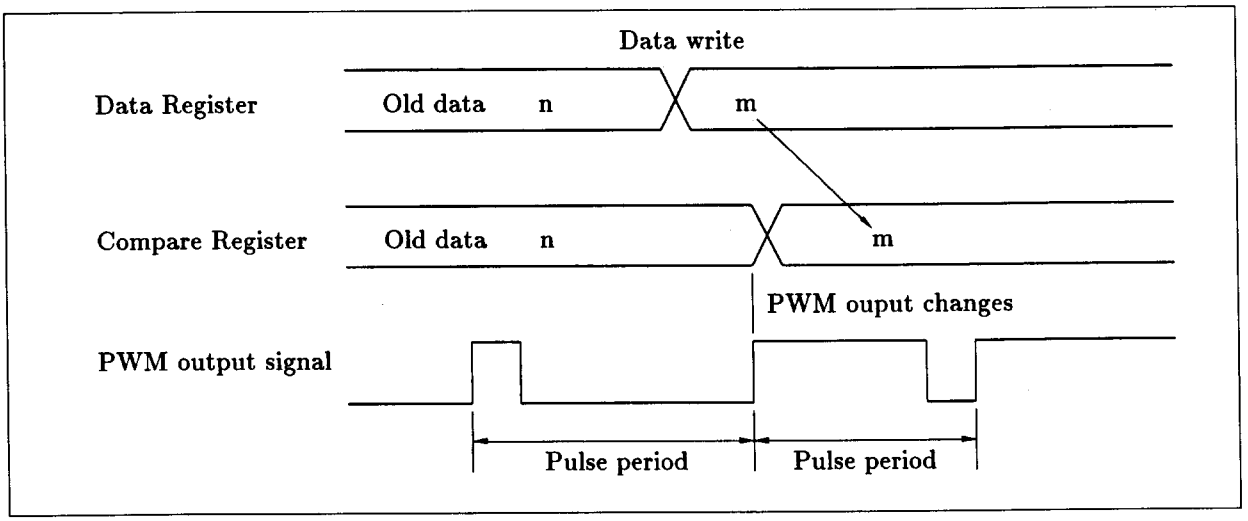


Fig 4-17. 8-bit Data Transfer Timing

• 8-bit PWM Pulse Output

8-bit PWM pulse output sends out pulse frequency (27.2μs/ 9.408MHz that is 2^8 times of PWM clock (2/ f_{EX}) and PWM pulse of pulse width that is decided on the value by PWM data register.

By integrating this PWM pulse through the low-pass filter external, it is possible for DC voltage with 8-bit resolving-power to be converted.

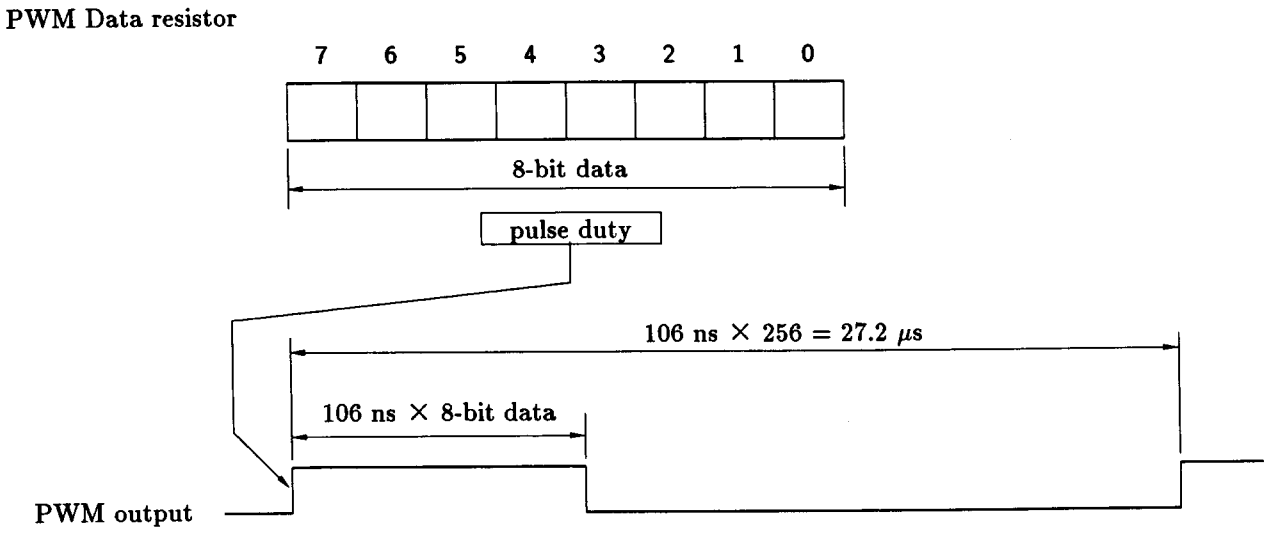


Fig 4-18. 8-bit PWM Pulse Output

(2) 12-bit PWM pulse output

First, the upper 8-bits of the 12-bit output data must be written to the PWM Data Register High (PWM3H, PWM4H), and the lower 4-bit as well as the PWM output polarity must be written to the PWM Data Register Low (PWM3L, PWM4L). Next, clear to "0" the bit in the Port E/SWP, PWM output selection register that corresponds to the channel to be output. By switching the port to PWM, PWM pulses will be output. This bit will be "0" after reset. The PWM output is free-running, so PWM pulses will be output continuously.

Data transfer from the data register to the compare register is performed by writing to the PWM Data Register High. The timing to modify PWM outputs is within a pulse period 2^8 times the PWM clock ($2/f_{EX}$).

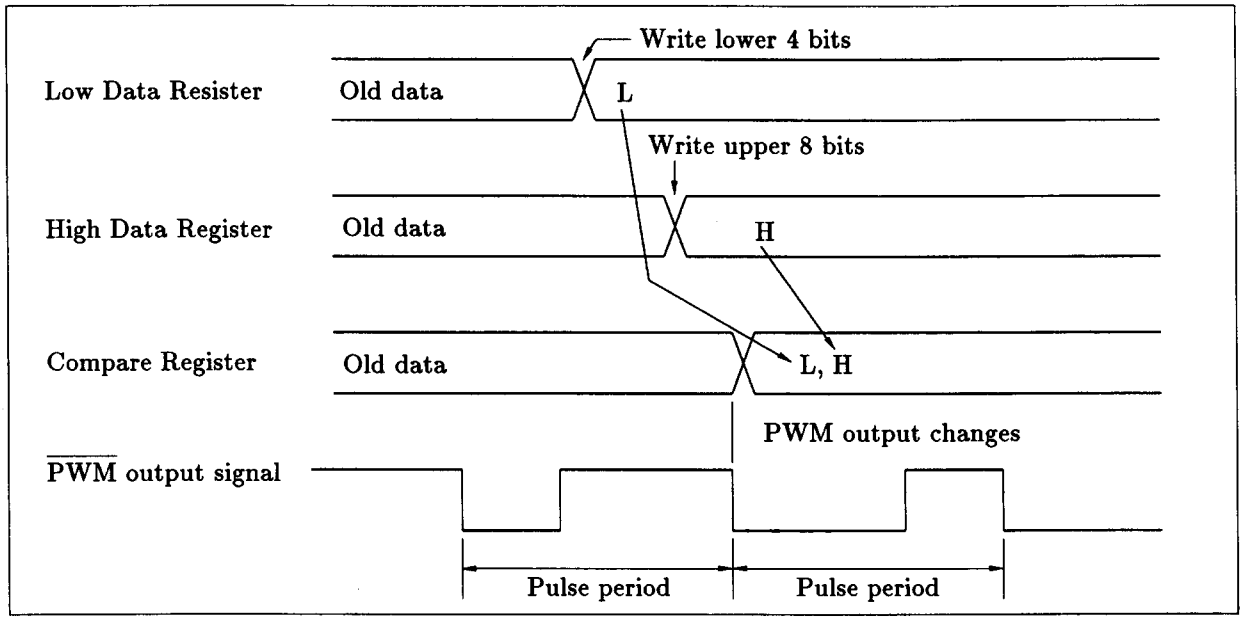


Fig 4-19. 12-bit PWM Data Transfer Timing

12-bit PWM pulse output

The pulse width of the 12-bit PWM pulse output is determined by the PWM data register value and a pulse period (27.2μs/ 9.408MHz) of 2^8 times the PWM clock (2/ f_{EX}). It has a conversion period (435μs/ 9.408MHz) of 2^{12} times the PWM clock.

By integrating the PWM pulses though an external low-pass filter, they can be converted to a DC analog voltage with 12-bit resolution. One conversion period is 16 cycles of 27.2μs (9.408MHz) PWM pulses. The total duty in one conversion period is calculated as follows :

Total duty width = 2/ f_{EX} × (12-bit PWM data value)

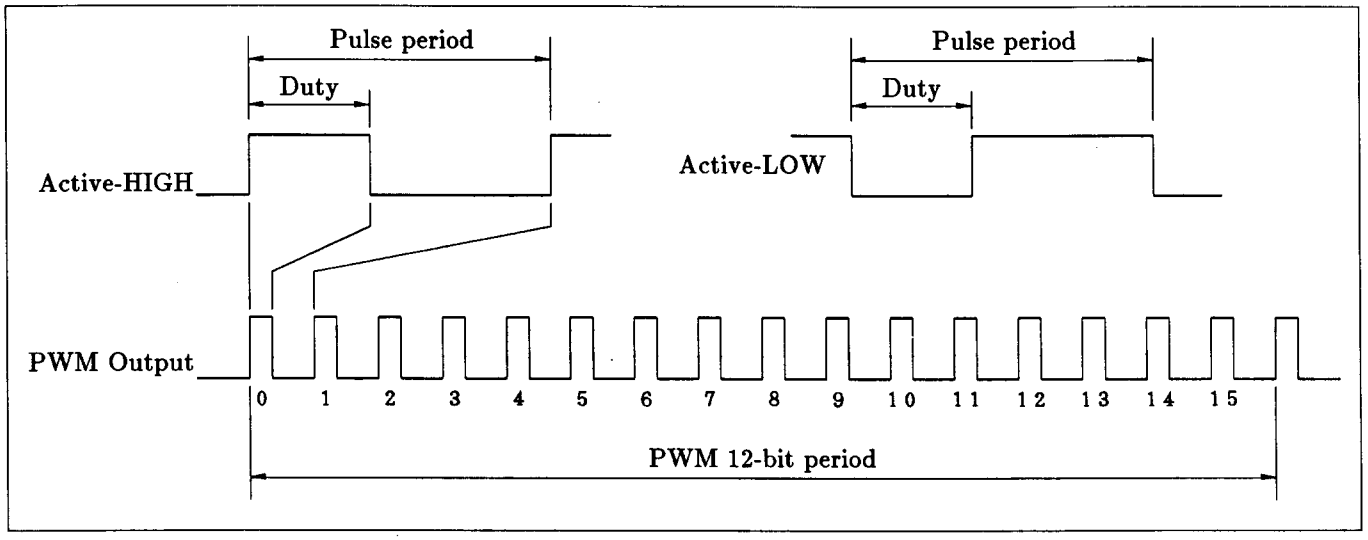


Figure 4-20. 12-Bit PWM Pulse Output

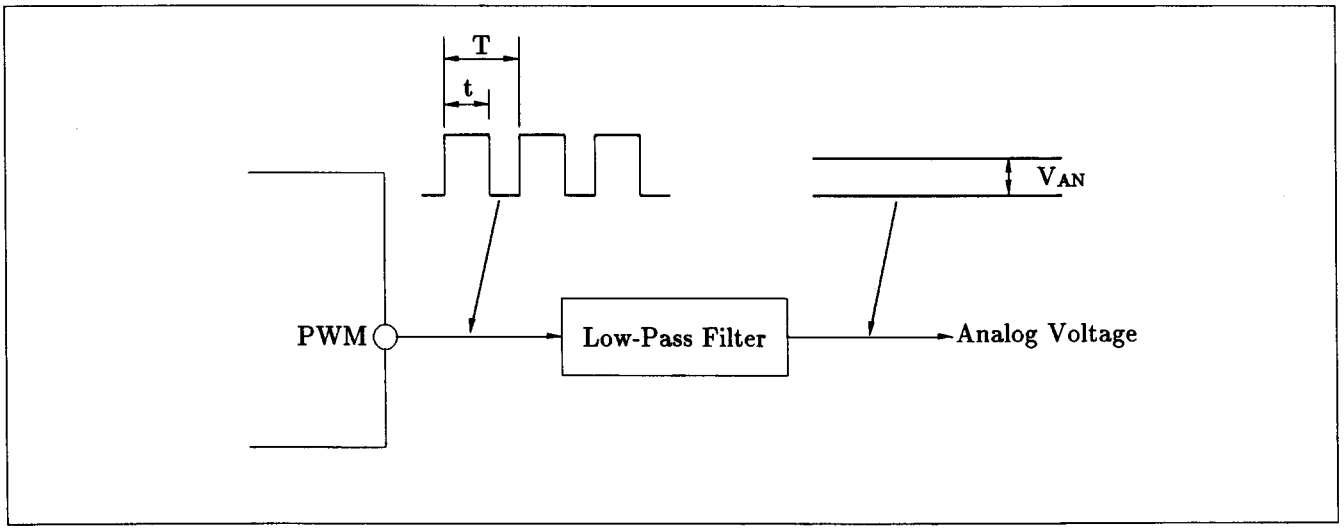


Figure 4-21. External Circuit for PWM Output Mode

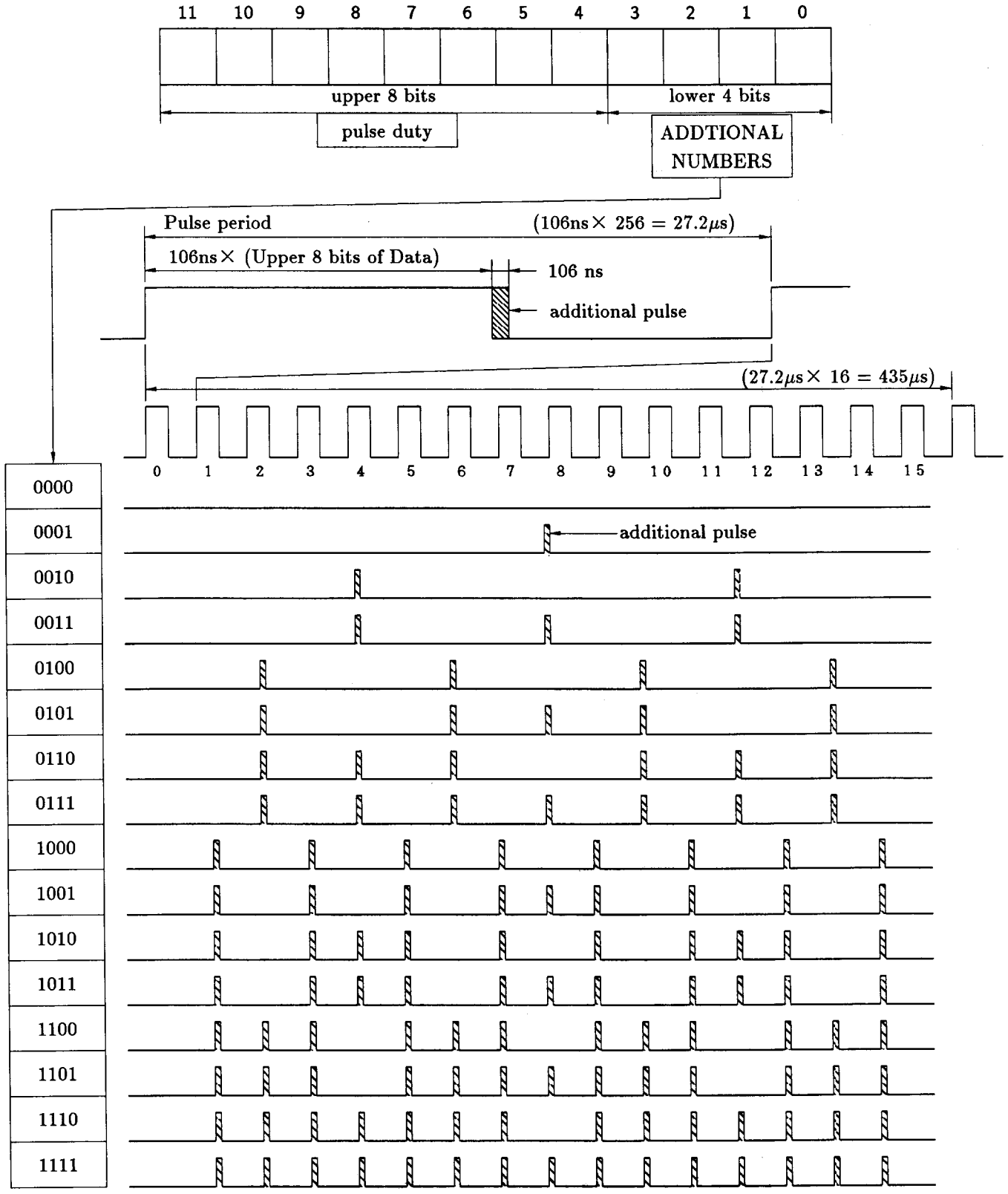


Fig. 4-22 Relation Between PWM 12-Bit Data and Pulse Output Waveform (polarity : active - HIGH)

5. DIGITAL FADE IN/OUT

Figure 5-1 shows the fade-in/out circuit during recording and playback.
The system is operated by IC306 CXD1136Q (digital filter).

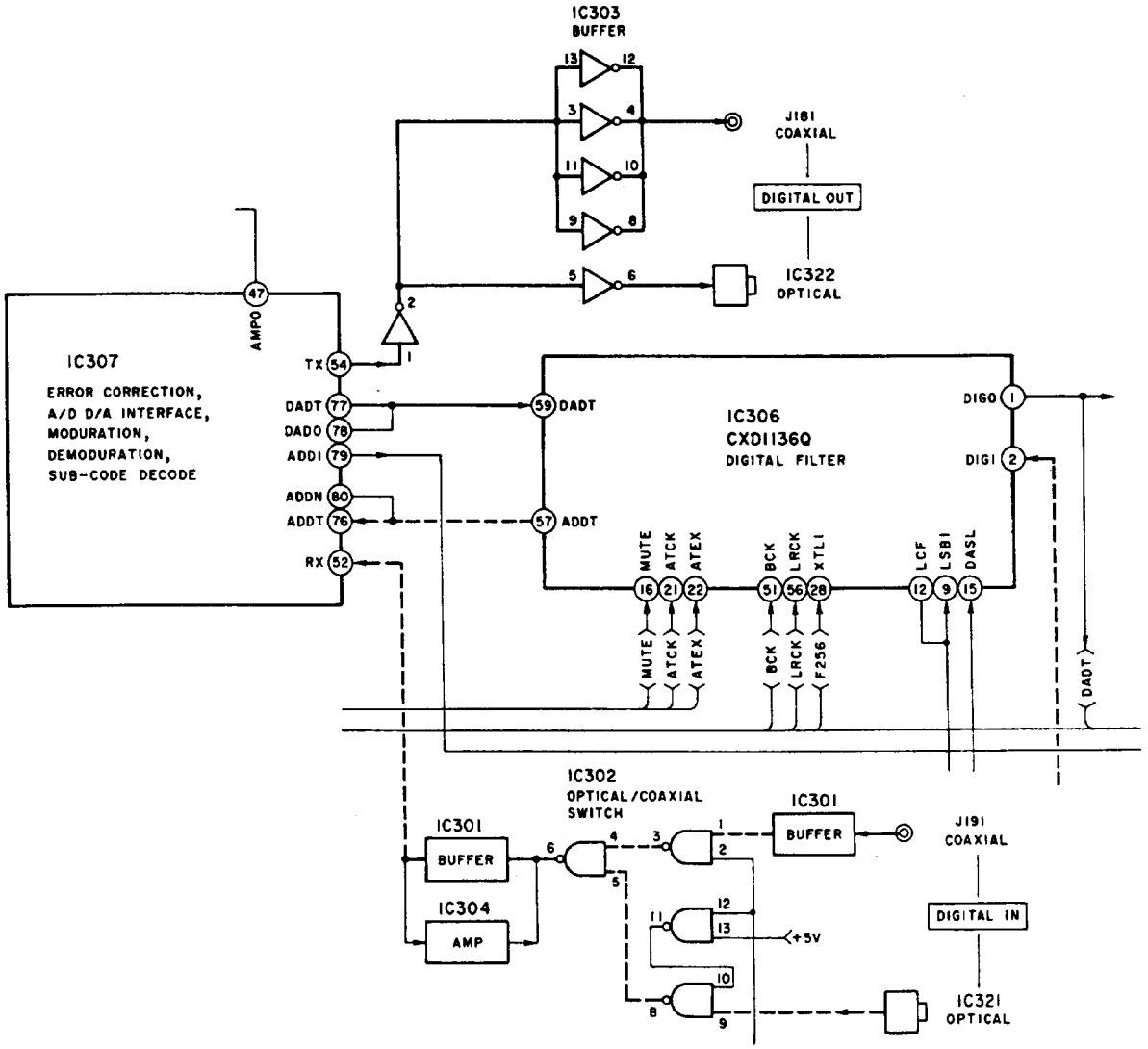


Figure 5-1. Digital Fade IN/OUT Circuit

CXD1136Q includes digital filter functions such as double oversampling, level detection and digital volume. The digital volume function is used to direct the fade-in/out operation.

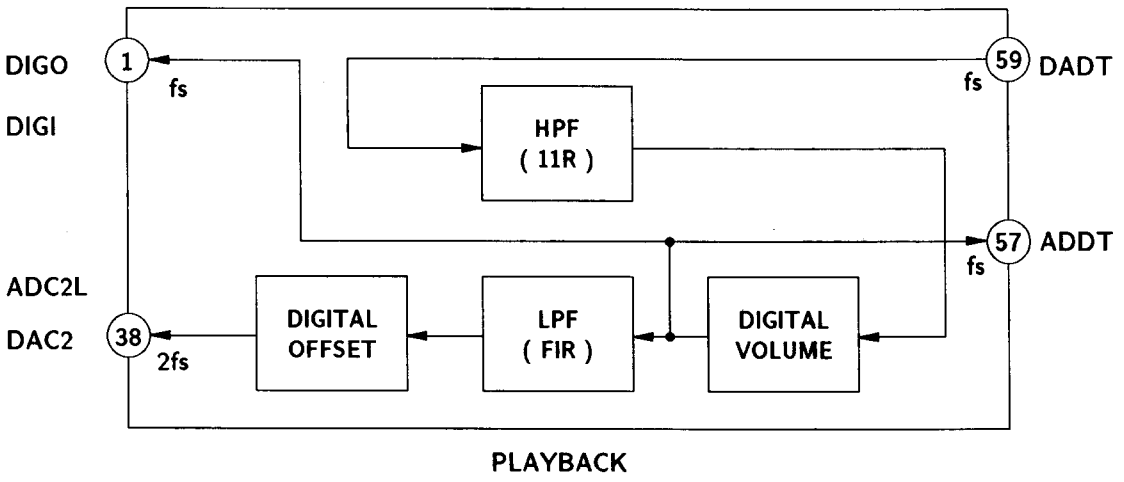
Pin 16 (MUTE) is a control signal terminal for the muting operation ('H' = MUTE ; 'L' = MUTE CANCEL).

Pin 21 (ATCK) is the level-setting clock for controlling the level in accordance with the number of clocks input.

When pin 22 (ATEX) turns 'H', muting operates at the internal clock ; when it turns 'L', muting is operated by the ATCK clock on pin 21.

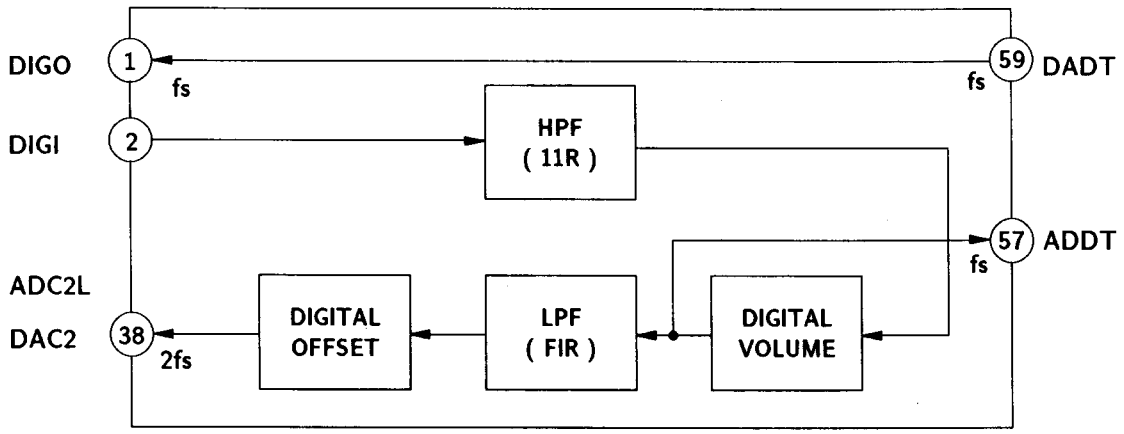
The fade-in/out operation is directed in accordance with the control signal fed to these input terminals.

Figures 5-2 and 5-3 show the internal status of CXD1136Q (digital filter) during playback and recording respectively.



PLAYBACK

Figure 5-2. Playback Operation



RECORDING

Figure 5-3. Recording Operation

Fade-in/out during playback

Figure 5-4 shows the timing chart of the fade-in/out operation during playback.

The fade-in/out timing depends on the time-setting point (0.2~15 s).

The line output is muted during the pause mode.

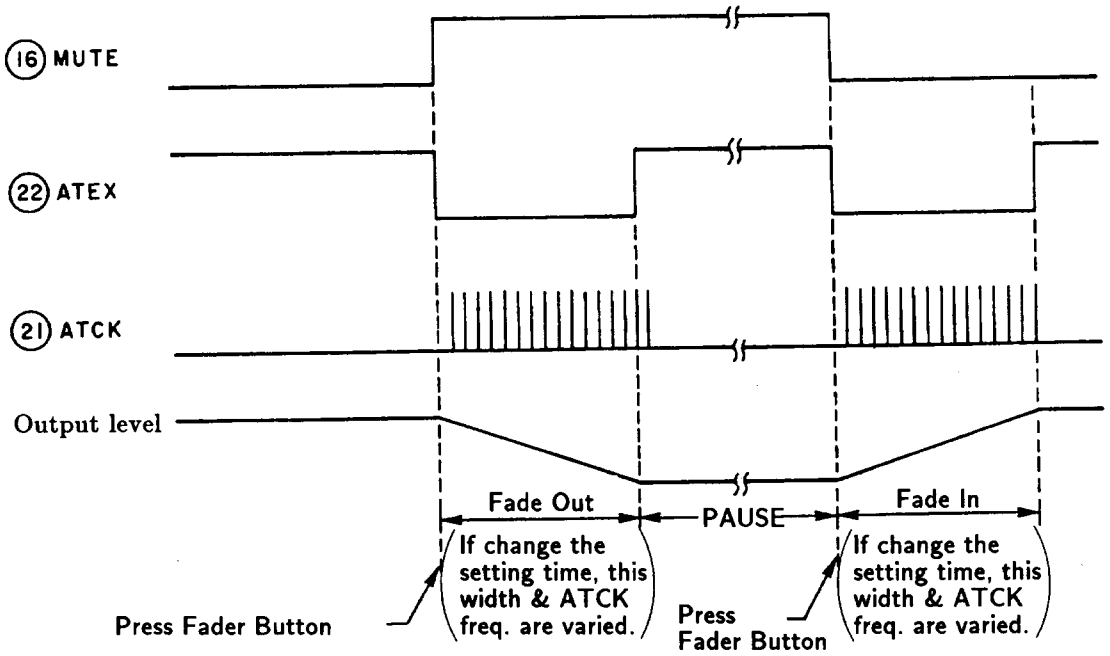


Figure 5-4. Fade-in/out timing during playback

Fade-in/out during recording

Figure 5-5 shows the timing chart of the fade-in/out operation during recording.

The difference with the fade-in/out operation during playback is that the line output is required during the pause mode, and that the operation starts just after the fade-out returns the line output to its previous level and just before the fade-in mutes the line output.

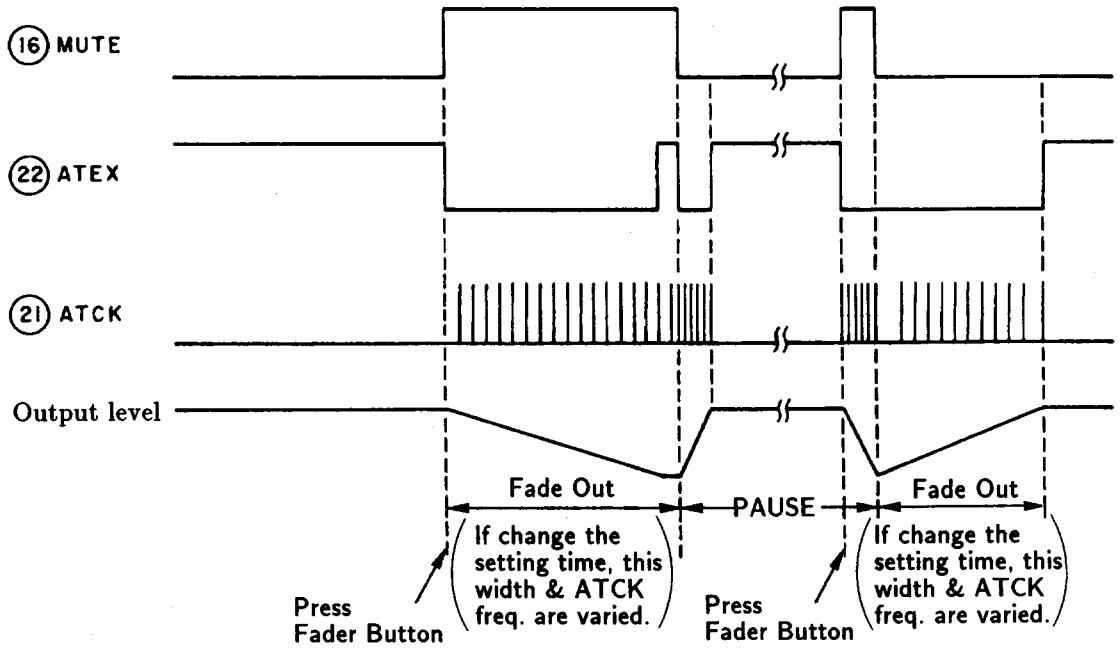


Figure 5-5. Record Fade IN/OUT Timing

6. LONG-PLAY MODE AND NON-TRACKING PLAYBACK

Table 1-2 shows that the tape speed and the number of drum rotations in the long-play mode (32k LP) are half the ones of the standard mode.
In figure 6-1 the timings of the long-play and the standard modes during recording are compared.

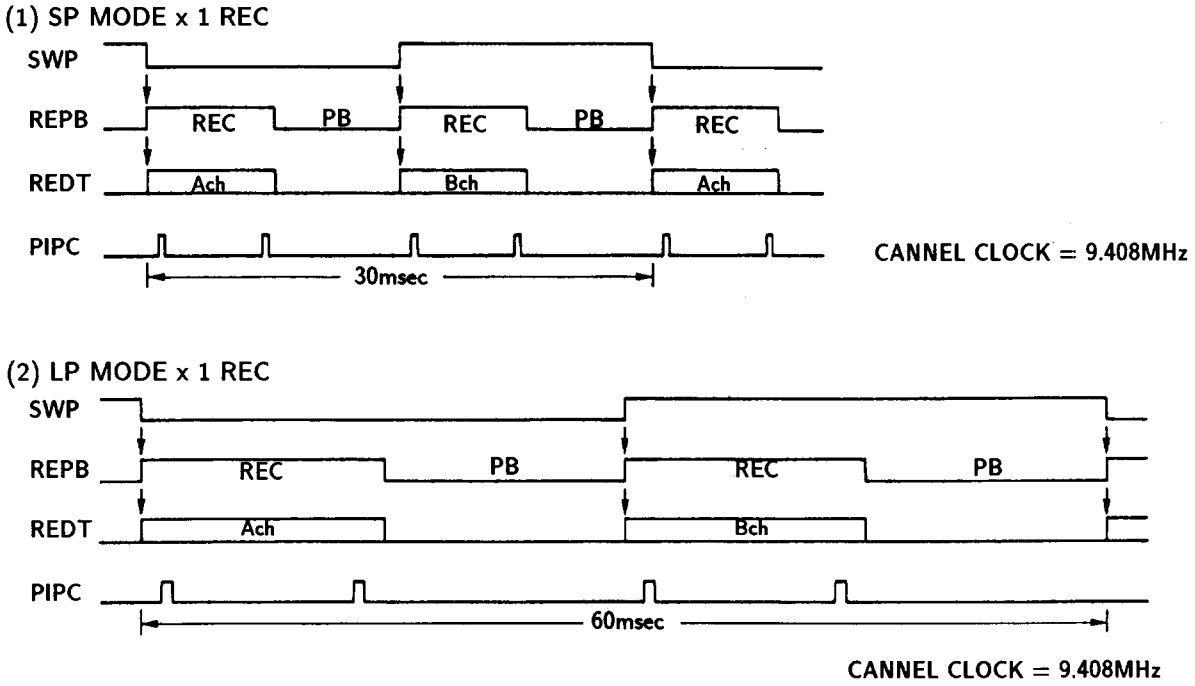


Figure 6-1. Recording Timing

REPB is the REC/PB switching signal whereas PIPC is the ATF pilot signal indicating the recording area. Feeding the PIPC signal to CXA1045 (RF AMP) allows to vary the recording level of the ATF pilot signal.
By halving the number of drum rotations, the head's playback output is reduced accordingly when playing back the track signals. Due to this, system noise relatively increases, thus deteriorating the error rate.
As the RF EQ circuit and the PLL constant have a different transmission rate, a modification is necessary.
It is shown in table 6-1 that during recording in the standard mode the number of drum rotations amounts to 2000 rpm ; during playback the data is transmitted at the standard 9.4 Mbps rate.

	Long play mode (LP)	Standard mode (SP)
Record	N = 1000 Vt = 4.075 R = 4.704	N = 2000 Vt = 8.150 R = 9.408
Playback	N = 2000 Vt = 4.075 R = 9.408	N = 2000 Vt = 8.150 R = 9.408

note) N : Drum rotation (rpm)
Vt : Tape sending (mm/sec)
R : Transmission rate (Mbps)

Table 6-1

As the number of rotations has doubled and the head is slightly slanting and off-track (refer to figure 6-2), the playback output will be decreased.

Nevertheless, the track is being read twice-hence NT (non-tracking) reading. The better data of both readings are selected to ensure a plausible error rate.

In the long-play mode, the tape speed is halved as well, both during recording and playback. Discrimination between normal speed and half speed is taken care of by S703 on recording, and by ID2 and ID4 of the main ID address on playback (refer to figure 6-3).

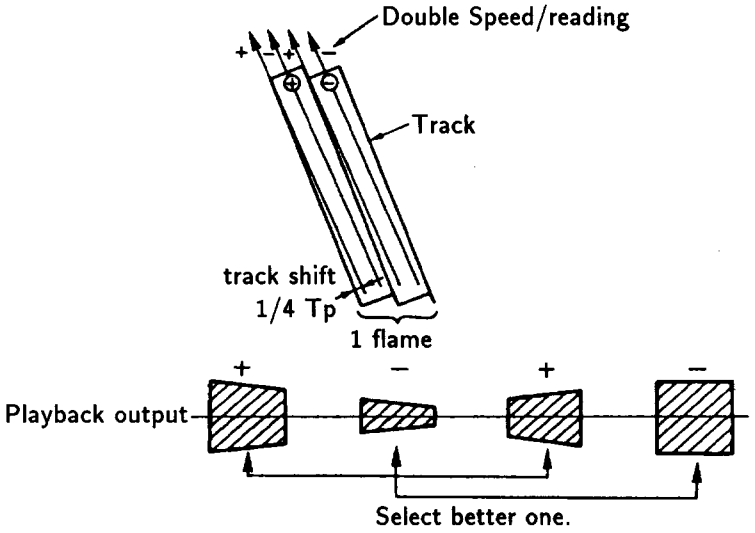


Figure 6-2. Double read-out playback

SYNC	Main ID		Main	Main Data (Dij, Pij, Qij) 256 bits (32 symbol)			
	W1	W2	Parity				
8 bits	8 bits	8 bits	8 bits	8 bits	8 bits	.....	8 bits

i = 0, 1, 2, ... 127
j = 0, 1, 2, ... 31

1 block = 8+8+8+8+8×32 = 288 bits

Main ID															
W1 (sub code)								W2 (block address)							
B7	B6	B5	B4	B3	B2	B1	B0	B7	B6	B5	B4	B3	B2	B1	B0
ID 0	0	ID1		FRAME address				0	X	X	X	X	0	0	0
ID2		ID3		〃				0	X	X	X	X	0	1	0
ID4		ID5		〃				0	X	X	X	X	1	0	0
ID5		ID7		〃				0	X	X	X	X	1	1	0

Even number Address Block

ID1 ~ ID6 has to be recorded

Each data ; Each FRAME
16×2 = 32 multi-writing

Figure 6-3.

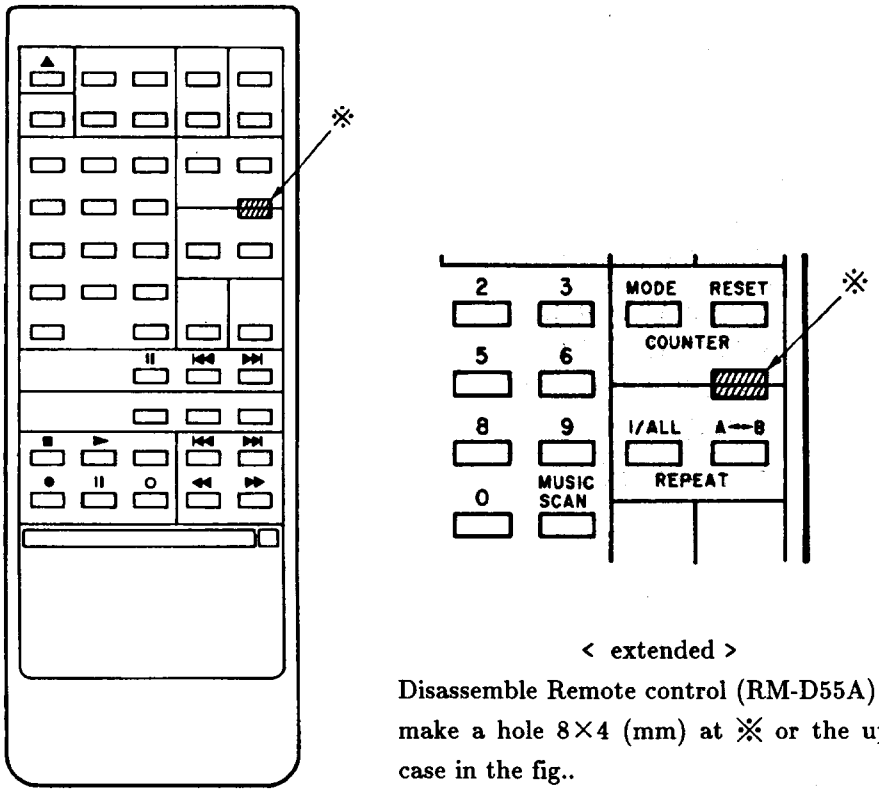
	Usage	Bit assignment
ID1	Einphasis	B5. B4 0 0 : Off 0 1 : 50/ 15 μsec
ID2	Sampling frequency	B7. B6 0 0 : 48 kHz 0 1 : 44.1 kHz 1 0 : 32 kHz
ID3	Number of channel	B5. B4 0 0 : 2 channels 0 1 : 4 channels
ID4	Quantization	B7. B6 0 0 : 16 bits linear 0 1 : 12 bits non linear
ID5	Track pitch	B5. B4 0 0 : Normal track mode 0 1 : Wide track mode
ID6	Digital copy	B7. B6 0 0 : Permitted 1 0 : Prohibited 1 1 : Permitted only for the first generation
ID7	Pack	B5. B4 Pack contents

Figure 6-2. BIT ASSIGNMENT OF ID1 ~ ID7 and subcode format of main ID

note) Long play mode (32k-LP) : ID2 = 10 (32kHz)
ID4 = 01 (12-bit non linear)

6-1. Test Mode

The DTC-55ES has a test-mode facility (refer to the service manual) which allows to display the internal state of the system control CPU.
In order to implement the test-mode facility, the remote control needs to be modified as shown in figure 6-4.
Depressing the newly installed button (TEST DISP) changes the normal display shown in figure 6-5 into the test display. The internal information of the display tube (1~11) is displayed in 4 bits (16 hex). A display '-' whereas F displays nothing.



< extended >
Disassemble Remote control (RM-D55A) and make a hole 8×4 (mm) at ※ or the upper case in the fig..

Figure 6-4. RM-D55A (Modified)

6-1-1. TEST DISPLAY I

Depress the TEST DISP button in the normal display mode once.

DISPLAY POSITION	BIT	CONTENTS	
②	0 1 2 3	CASSETTE COMPARTMENT OUT SW (ACTIVE HI) CASSETTE COMPARTMENT LOCK SW (ACTIVE HI) MIS-ERASE PROTECTION CLICK (HI : RECORD-ABLE) CASSETTE IN-SW (ACTIVE HI)	10M
③	0 1 2 3	ROTARY ENCORDER STOP POSITION ROTARY ENCORDER FWD POSITION LIMIT SW (H : UNLOAD POSITION) ———————————	M
④	0 1 2 3	CASSETTE COMP. ABNORMAL LOADING ABNORMAL END-SENSER ABNORMAL TRANSISION ABNORMAL	10S
⑤	0 1 2 3	DRUM ABNORMAL CAPSTAN ABNORMAL T-REEL ABNORMAL S-REEL ABNORMAL	S
⑥⑦		DPG SETTING	PGM
⑧⑨		MECH OPERATION MODE	AMS

Table 6-3. Contents of test display I

Display position ⑧, ⑨	Contents	Display ⑧, ⑨	Contents
* *	FWD (SP)	* 8	STOP (SP)
4 0	FWD (LP)	4 8	STOP (LP)
* 6	FF	1 8	LOAD
* 4	FF	1 C	UNLOAD
1 6	REW	* 9	FWD (SP) PAUSE
1 4	REW	4 9	FWD (LP) PAUSE
* —	REC (SP)	* b	REC (SP) PAUSE
4 —	REC (LP)	4 b	REC (LP) PAUSE

* : no display

Table 6-4. Display of mechanical operation mode

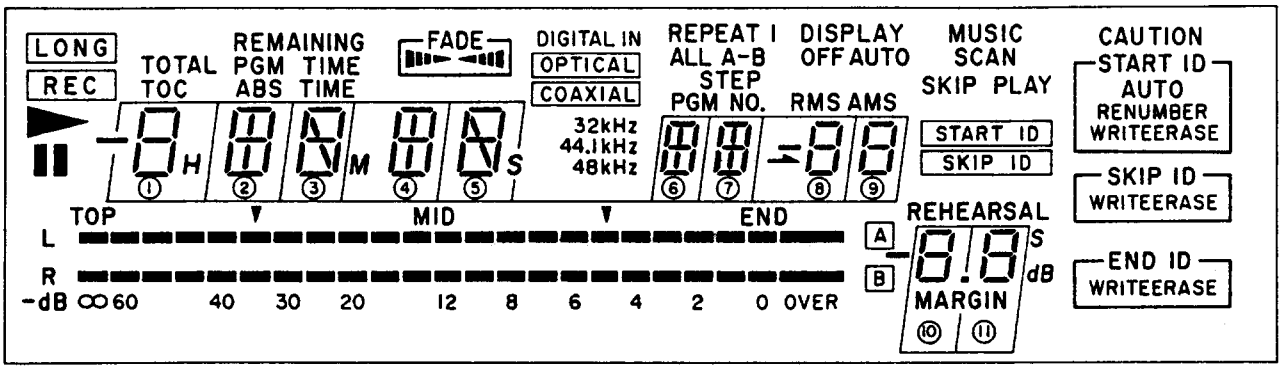


Figure 6-5. Digits of the Display used in the Test Mode

Fig 6-5. Display positions

6-1-2. Test Display Ⅱ

Key in the following sequence in the normal display mode : '8' → 'NUMERIC KEY' → 'TEST DISP'. Then display the key information by keying in '8' → '4' → 'TEST DISP'.

Table 6-5. Contents of test display Ⅱ

	CONTENT									
KEY INFORMATION DISPLAY "3" "4" "TEST DISP"		①	②	③	④	⑤	⑥	⑦	⑧	⑨ ⑩ ⑪
	0	SK-WR	ST-WR	REPEAT	FADER	ED-WR	AUTO	◁◁	⏏	SIRCS DATA
	2	SK-ER	ET-ER	SKIPPLAY	C. RESET	ED-ER	RENUMBER	▷▷	□	
	4	7	4	M. RESET	C. MODE	CLEAR	1	○	▷	
	6	8	5	OPTICAL	T. PLAY	ϕ	2	▯▯	⏮	
	8	9	6	COAXIAL	T. REC	H. SCAN	3	●	⏭	
	-	—	—	ANALOG	T. OFF	—	—	—	—	
ALL DISPLAY ON "8" "5" "TEST DISP"	FL ALL SEGMENT'S ON									

DRUM OPERATION TIME DISPLAY "8" "7" "TEST DISP"	①	②	③	④	⑤	⑥	⑦	⑧	⑨
	1,000H	100H	10H	1H	—	10 MIN	MIN	10SEC	SEC

CASSETTE COMPARTMENT IN AND OUT OPERATION (times) DISPLAY "8" "8" "TEST DISP"	①	②	③	④	⑤	⑥	⑦	⑧	⑨
	—	100,000	10,000	1,000	100	10	1	—	—

6-1-3. Test Display Ⅲ

Enter code + '10KEY " 10KEY " 10KEY " 10KEY " TEST KEY " TEST KEY '

Table 6-6 Contents of test display Ⅲ

CONTENTS	DISPLAY POSITION				
No. KEY input	②	③	④	⑤	Bit
Port "A", "B" In/Output data 1 1 6 0	ATF S2 75P ATT EXT 76P ATF S3 77P MUTE 2 78P	MUTE 1 79P X DTR 80P — 1P — 2P	L PIN ON 3P REEL CCW 4P REEL CW 5P CAP DIR RVS 6P	PLN ON 7P PLN KICK 8P DRUM ON 9P DRUM DIR RVS 10P	3 2 1 0
Port "C", "D" In/Output data 1 1 6 1	COA/XOPT 11P DIG/XANA 12P REC/XPB 13P ATCK 14P	— 15P — 16P LE 17P LL 18P	D/A MUTE 19P L MUTE 20P TR MUTE 21P X DISP SL 22P	— 23P LIM SW 24P RE FWD 25P RE STOP 26P	3 2 1 0
Port "E", "F" In/Output data 1 1 6 2	SWP 63P D PWWM 64P C PWM 65P PWM R 66P	— 67P AGC PWWM 68P ER MON 69P X TEST 70P	T END 47P S END 48P CAS IN 49P REC EN 50P	CAS LCKED 51P CAS OUTED 52P LVL SYNC 53P ATF IN 54P	3 2 1 0
Port "G", "H" In/Output data 1 1 6 3	FG T 55P FG S 56P C FG 57P D FG 58P	D PG 59P D REF 60P MST CK 61P BP DT 62P	CAS M IN 27P CAS M OUT 28P T LED ON 29P S LED ON 30P	DISP SYNC 36P DISP DT 1 37P DISP D O 38P DISP CK 39P	3 2 1 0
MASTER SLAVE MODE BYTE 1 3 0 0	MASTER MODE BYTE D7 D6 D5 D4	 D3 D2 D1 D0	SLAVE MODE BYTE D7 D6 D5 D4	 D3 D2 D1 D0	 3 2 1 0
DIGITAL IN READ 1 3 0 1	DAT CATEGORY EMPHASIS 2 EMPHASIS 1 COPY PROHIBITED	DIGITAL/AUDIO PRO/CONSUMER XFCO "H" = NG UNLOCK ACT "H"			3 2 1 0

6-1-4. Test Mode I

Enter the following key sequence : '8' → 'NUMERIC KEY' → TEST DISP'. If no cassette is inserted, change the timer switch to the 0N position, keep both 'START ID WRITE' and 'SKIP ID WRITE' depressed, and switch the power switch on. Note that this procedure is only possible on this particular model.

TEST MODE I

OPERATION	CONTENT
COAXIAL IN MODE "8" "1" "TEST DISP"	FED TO BE COAXIAL IN, NO RELATION TO INPUT SELECT SW.
OPTICAL IN MODE "8" "2" "TEST DISP"	FED TO BE OPTICAL IN, NO RELATION TO INPUT SELECT SW.
ANALOG IN MODE "8" "3" "TEST DISP"	FED TO BE ANALOG IN, NO RELATION TO INPUT SELECT SW.
POWER ON TEST MODE "T. PLAY" " ST-ID WRITE + SK-ID WRITE " → POWER ON	TEST MODE, NO CASSETTE.

Table 6-7. Contents of test mode I

7. MECHANICAL TROUBLESHOOTING

This feature allows to check the mechanical operation of recording, playback, scan, and search. A forced stop or unloading will result when either one of these dose not comply with the standards.
When an abnormality is detected, the forced-stop/unload function may eject the tape without damaging the tape itself or the mechanical desk.
Both the tape and the complete set are protected against anomalies by this unique checking function. Refer to table 7-1 for more details.

Table 7-1

ANAMALOUS	CONDITION	PROCESSING AFTER SHOOTING
TRANSITION ABNORMAL	SOMETING COULD NOT HAPPEN HAS APPEARED. (FF → REC etc.)	NOT RECEIVE CAUTION EMITS
END SENSOR	DURING END-SHOOTING BOTH T/S SIDE END SENSERS. (PROBABILITY OF TAPE TEARING APART)	EXCEPT EJECT, KEYS ARE NOT RECEIVED. UNLOAD CAUTION EMITS
LOADING	WHEN WITHIN 4sec LOADING POSITION DIDN'T REACH ITS' OBJECT POSITION.	LOADING STOP CAUTION EMITS
CASSETTE COMPARTMENT	IF WITHIN 3sec CASSETTE COMP. HASN'T REACH ITS' OBJECTIVE POSITION.	CASSETTE STOP CAUTION EMITS
S REEL	WHEN S SIDE REEL SHOULD MOVE AT MECH MODE TIME, IF S SIDE REEL FG HASN'T BEEN INPUTTED FOR ABOUT 4sec.	STOP OPERATION
T REEL	WHEN T SIDE REEL SHOULD MOVE AT MECH MODE TIME, IF T SIDE REEL FG HASN'T BEEN INPUTTED FOR ABOUT 4sec.	STOP OPERATION
CAPSTAN	WHEN CAPSTAN SHOULD MOVE AT MECH MODE TIME, IF CAPSTAN FG HASN'T BEEN INPUTTED FOR ABOUT 200mS.	STOP OPERATION CAUTION EMITS
DRUM	WHEN DRUM SHOULD REVOLVE AT MECH MODE, IF DRUM FG HASN'T BEEN INPUTTED FOR ABOUT 200mS.	EXCEPT EJECT, KEYS ARE NOT RECEIVED. UNLOAD CAUTION EMITS

8. ROTARY ENCODER OPERATION

The DAT operation can be classified into three main mechanical modes : STOP, LOADING, and UNLOADING. These modes are selected by the rotary encoder which determines the pinch-roller/guide specifications in FWD and STOP. Its timings are shown in figure 8-1.

The rotary encoder dose not influence the unloading completion ; it is the limit switch (S902) that determines the position.

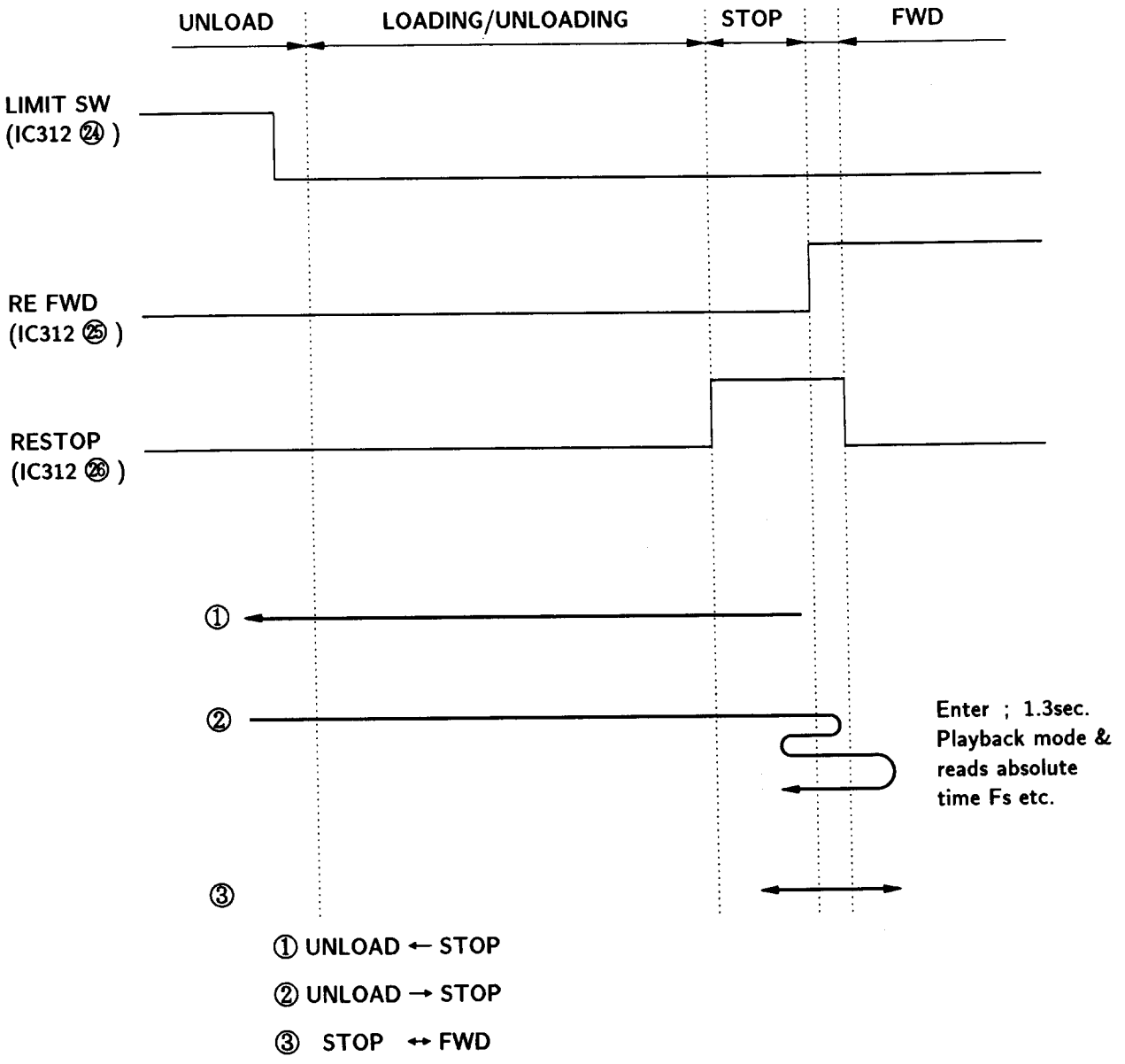


Figure 8-1. Timing chart of rotary encoder and limit switch

9. Mechanical Operation

9-1. locations/assignments of motor & switches

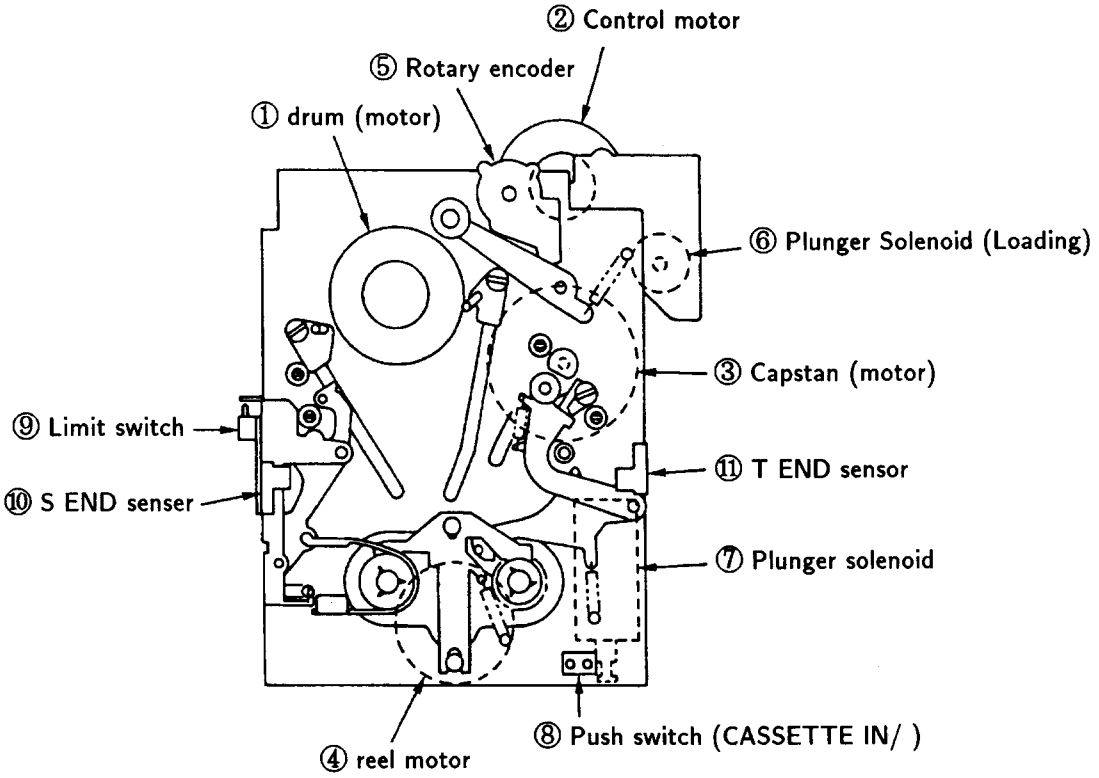


Fig. 9-1 Mech. on Mercator's projection

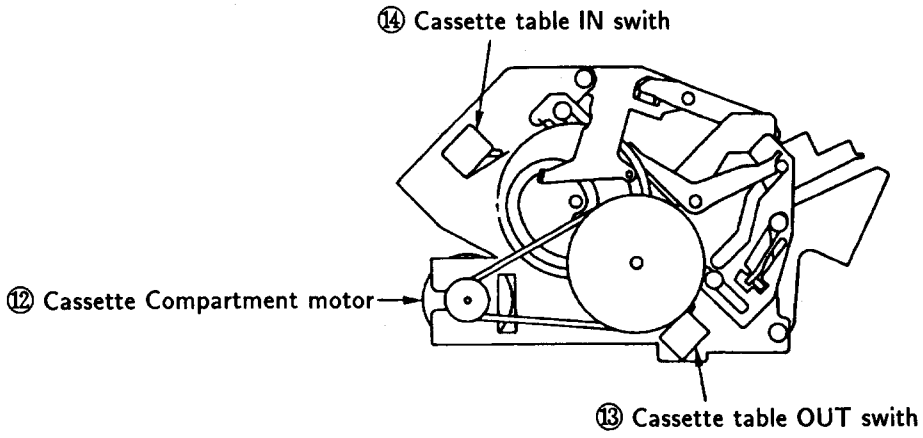
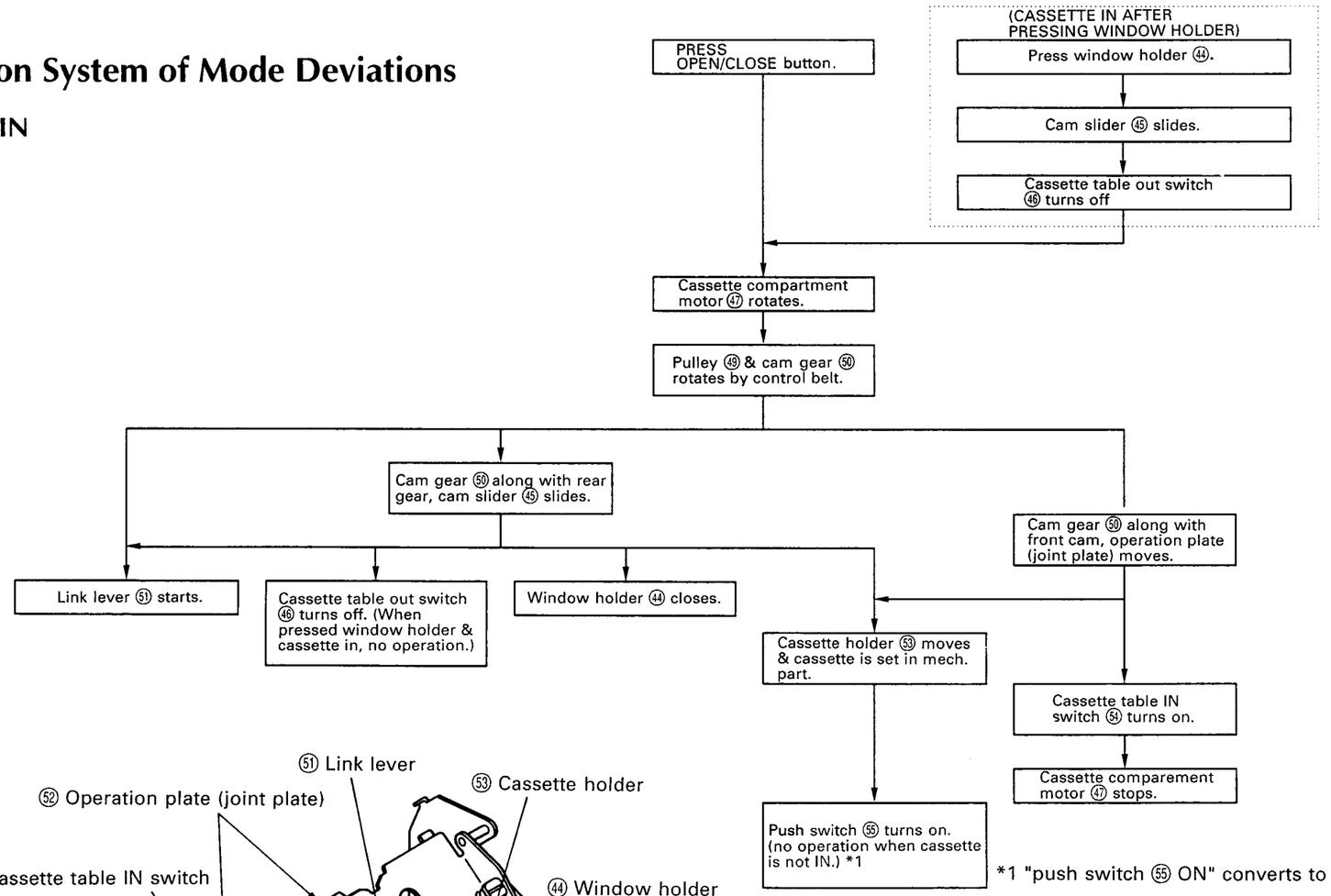
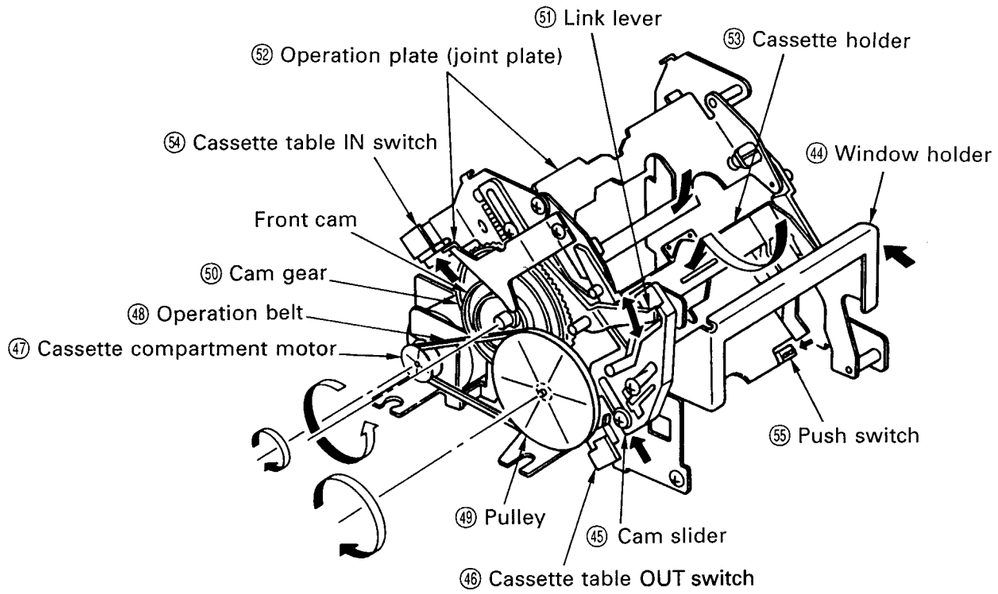


Fig. 9-2 Cassette Compartment of the left-sided

9-2 Operation System of Mode Deviations

9-2-1 Cassette IN





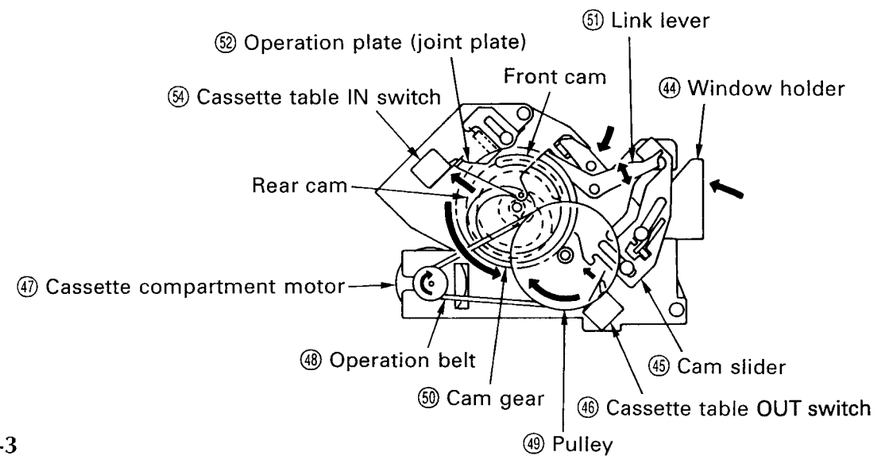
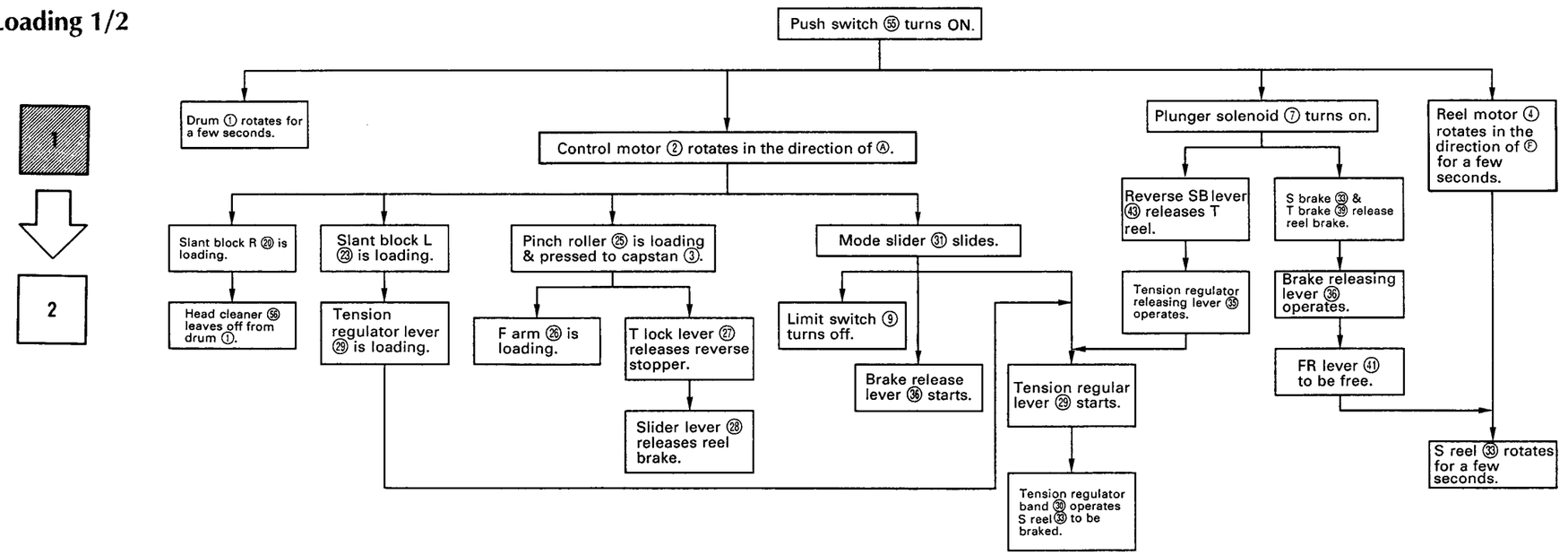
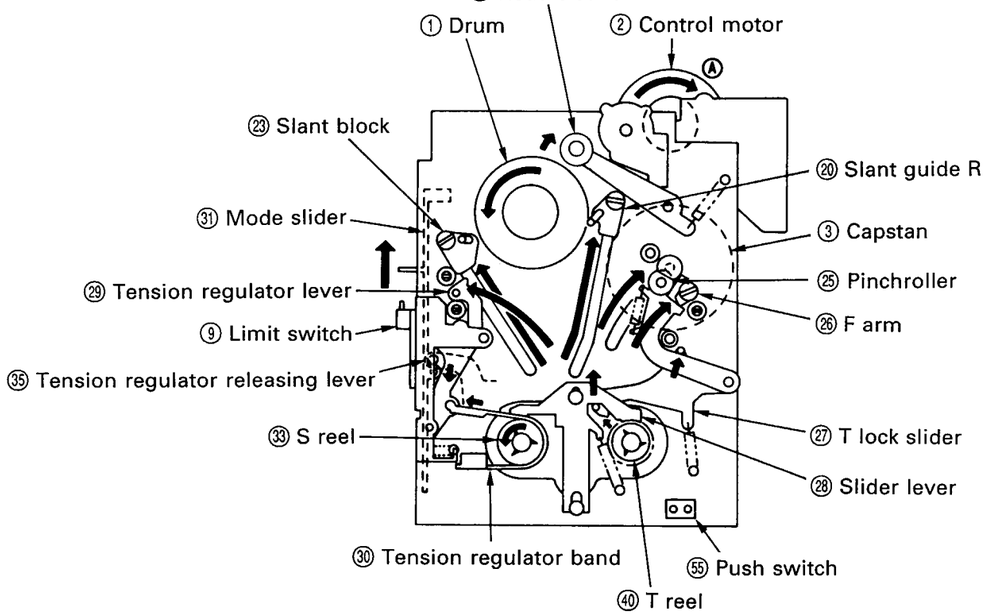


Fig. 9-3

9-2-2 Loading 1/2





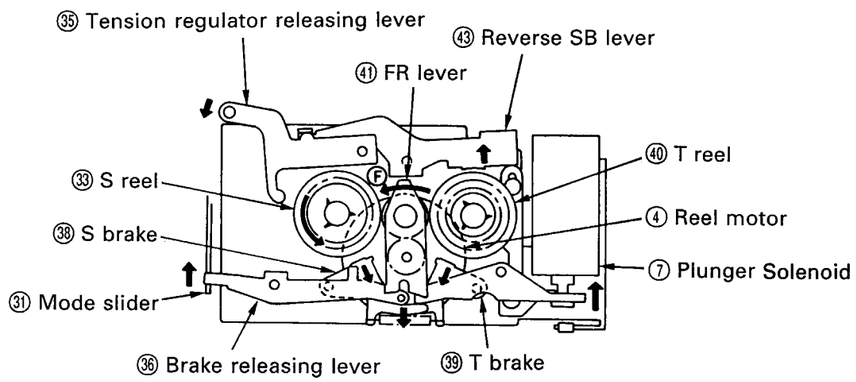
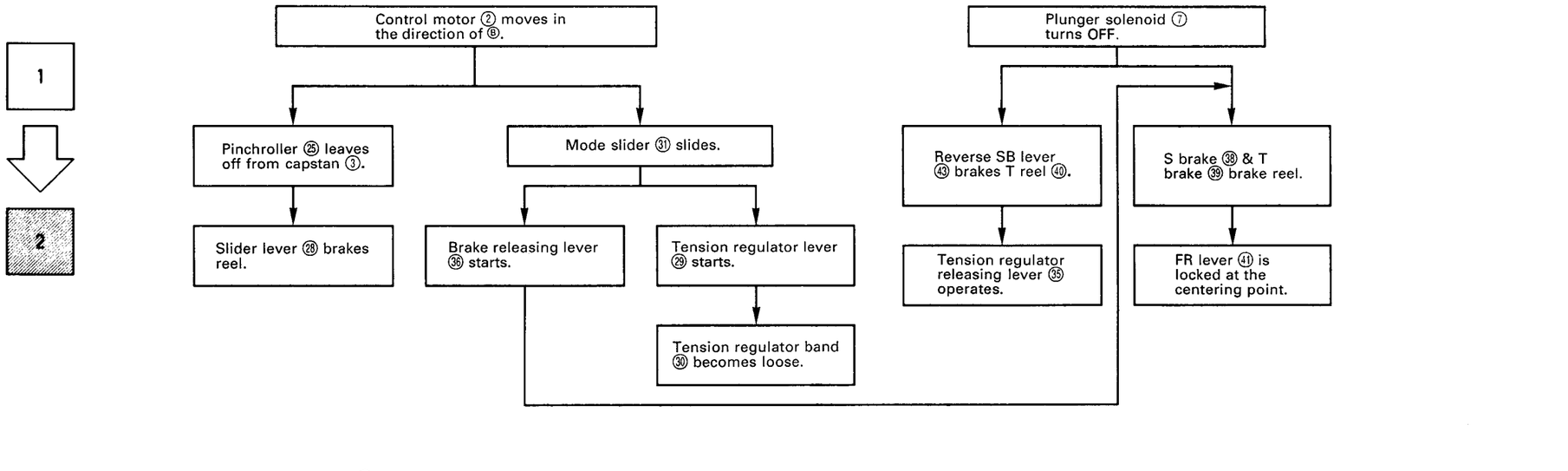
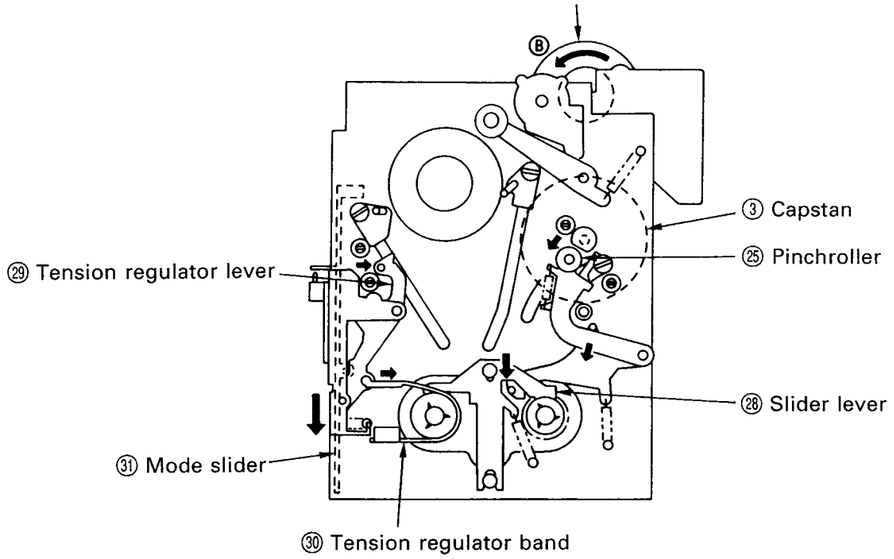


Fig. 9-4


1
2
Control motor ② moves in the direction of Ⓑ.
Pinchroller ㉕ leaves off from capstan ③.
Slider lever ㉘ brakes reel.
Mode slider ㉛ slides.
Brake releasing lever ㊱ starts.
Tension regulator lever ㉙ starts.
Tension regulator band ㉚ becomes loose.
Plunger solenoid ⑦ turns OFF.
Reverse SB lever ㊸ brakes T reel ㊵.
Tension regulator releasing lever ㉟ operates.
S brake ㊳ & T brake ㊴ brake reel.
FR lever ㊶ is locked at the centering point.


② Control motor
Ⓑ
③ Capstan
㉕ Pinchroller
㉙ Tension regulator lever
㉘ Slider lever
㉛ Mode slider
㉚ Tension regulator band

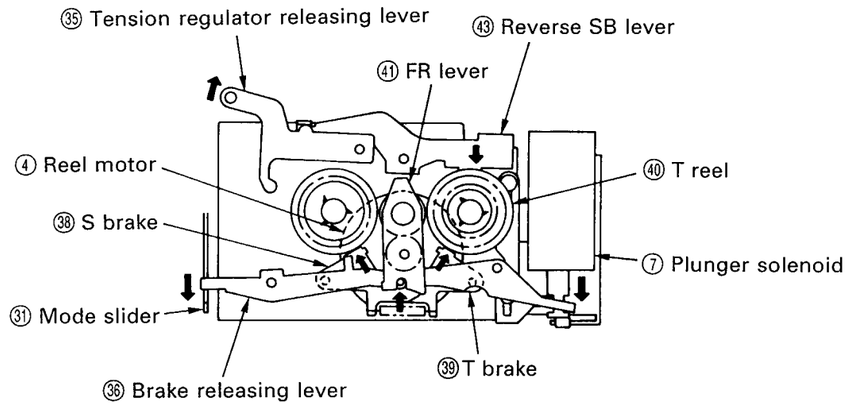
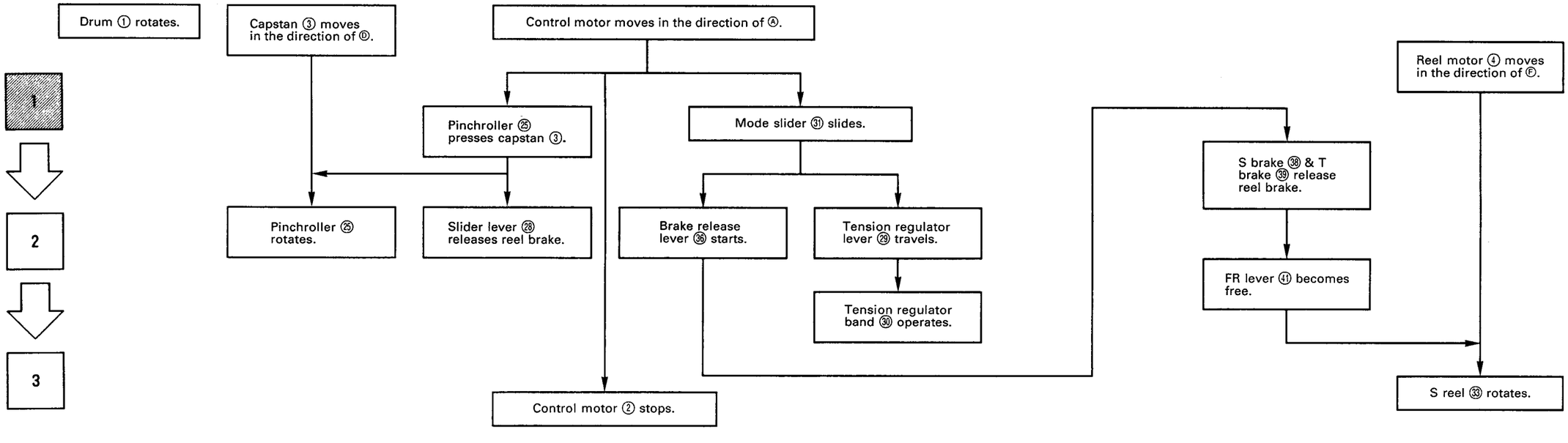
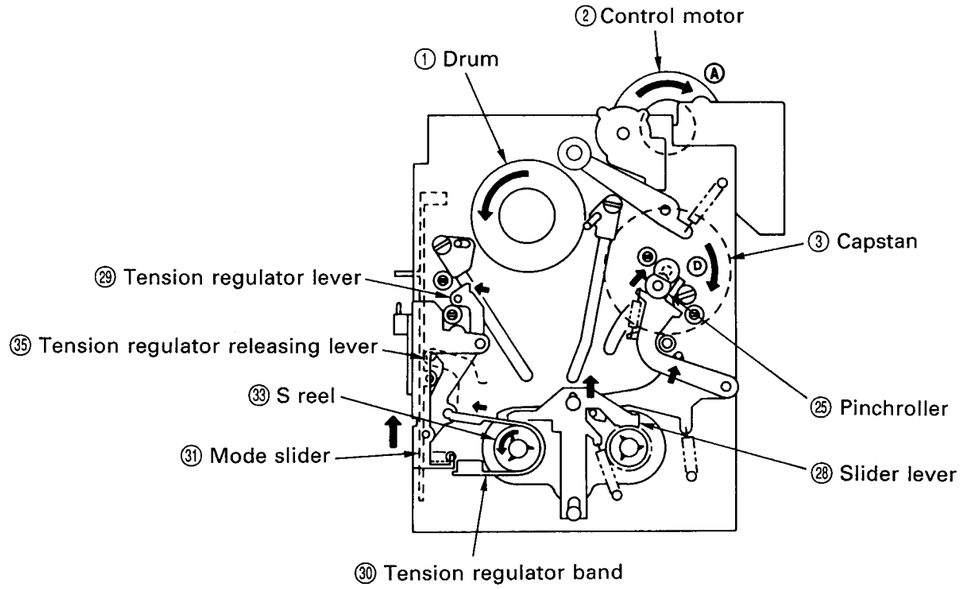

㉟ Tension regulator releasing lever
㊸ Reverse SB lever
㊶ FR lever
④ Reel motor
㊵ T reel
㊳ S brake
⑦ Plunger solenoid
㉛ Mode slider
㊴ T brake
㊱ Brake releasing lever

Fig. 9-5

9-2-2 Loading 2/2 (Tape signal read-in Operation)





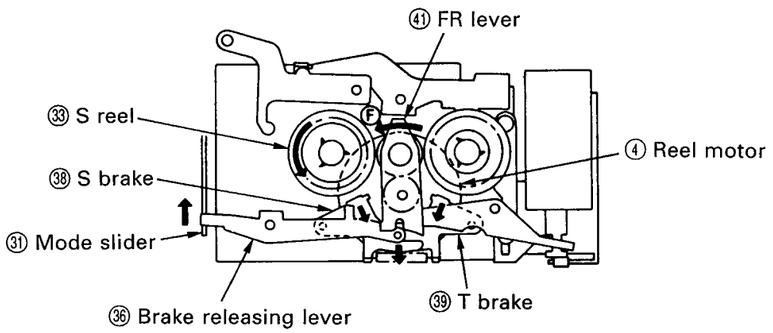
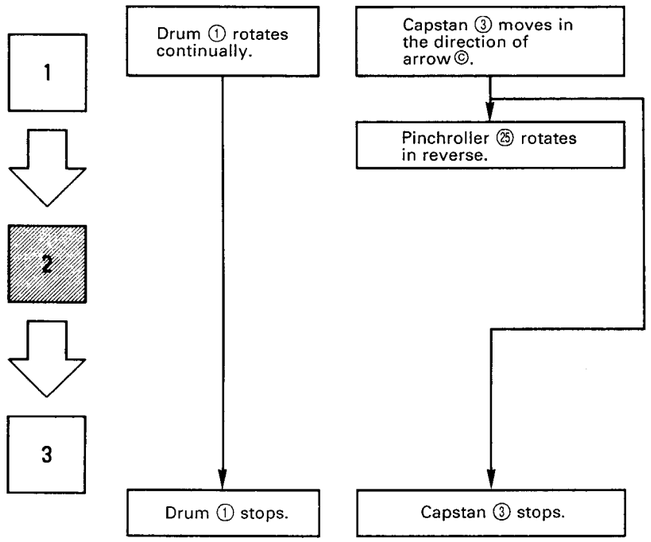
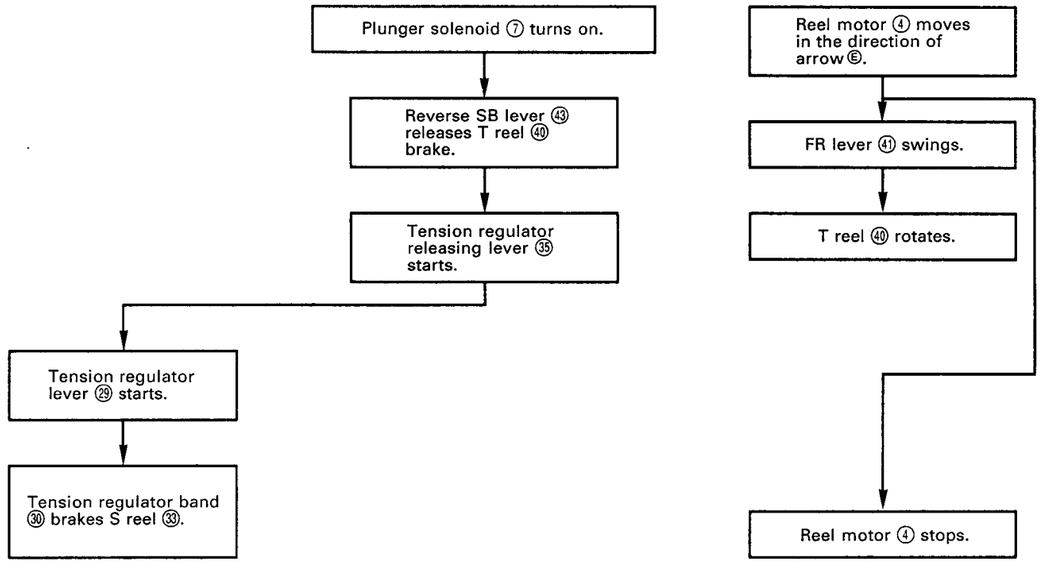
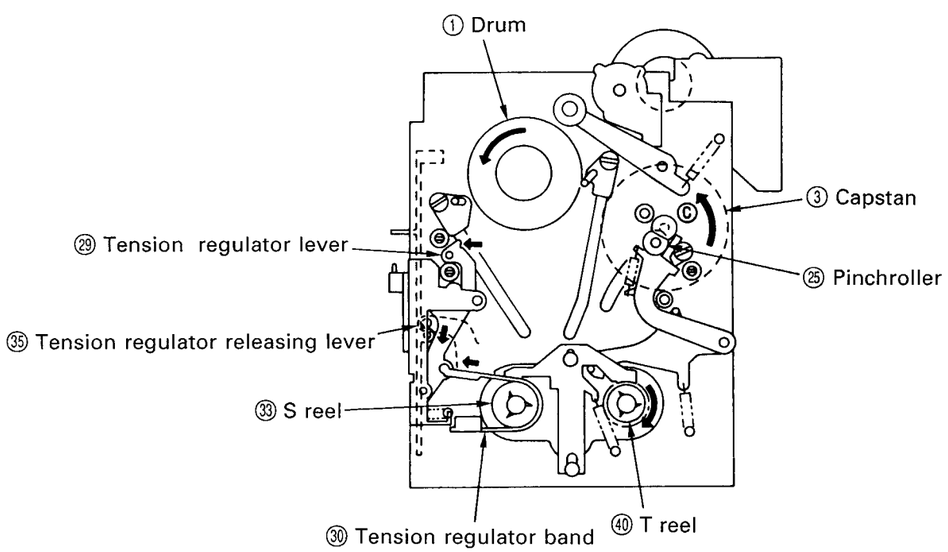


Fig. 9-6


1
2
3
Drum ① rotates continually.
Drum ① stops.
Capstan ③ moves in the direction of arrow Ⓒ.
Pinchroller ㉕ rotates in reverse.
Capstan ③ stops.


Plunger solenoid ⑦ turns on.
Reverse SB lever ㊸ releases T reel ㊵ brake.
Tension regulator releasing lever ㉟ starts.
Tension regulator lever ㉙ starts.
Tension regulator band ㉚ brakes S reel ㉝.
Reel motor ④ moves in the direction of arrow Ⓔ.
FR lever ㊶ swings.
T reel ㊵ rotates.
Reel motor ④ stops.


① Drum
③ Capstan
㉙ Tension regulator lever
㉕ Pinchroller
㉟ Tension regulator releasing lever
㉝ S reel
㉚ Tension regulator band
㊵ T reel

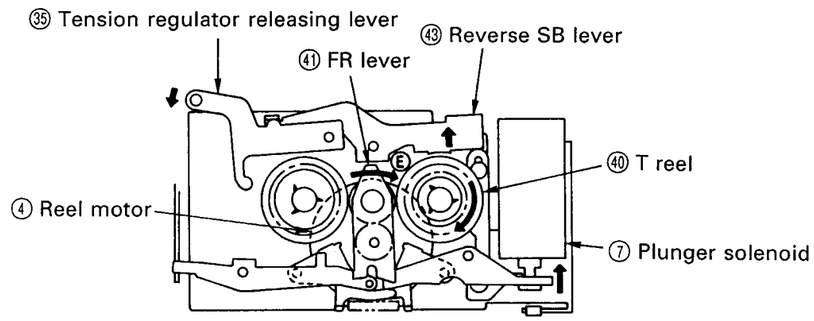
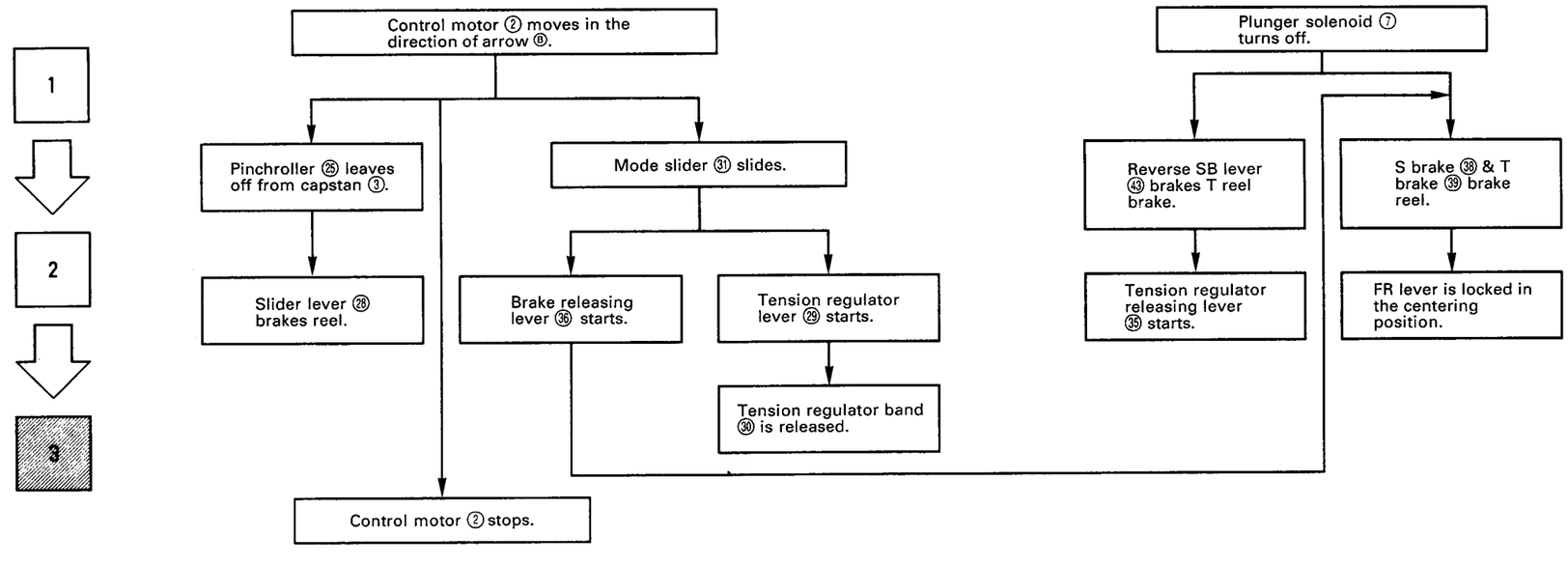
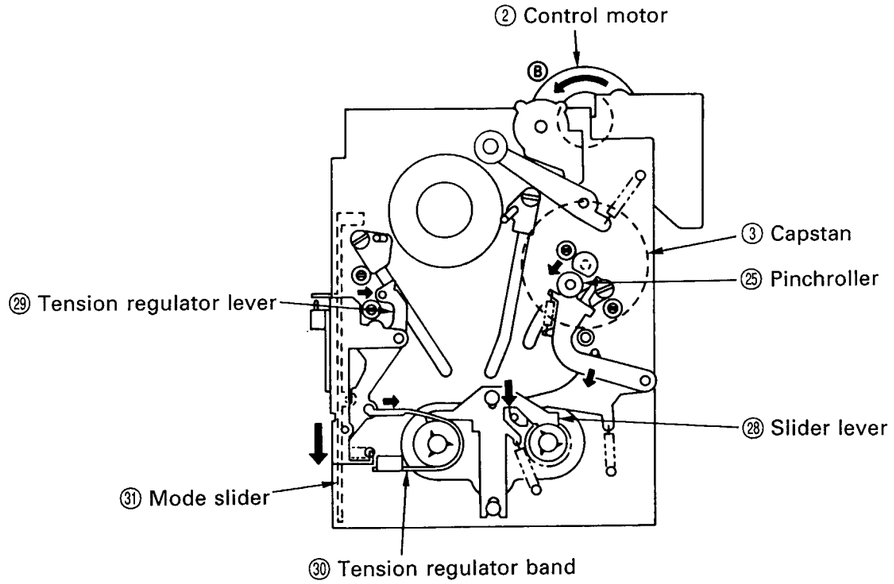

㉟ Tension regulator releasing lever
㊸ Reverse SB lever
㊶ FR lever
㊵ T reel
④ Reel motor
⑦ Plunger solenoid

Fig. 9-7


1
2
3
Control motor ② moves in the direction of arrow Ⓑ.
Pinchroller ㉕ leaves off from capstan ③.
Slider lever ㉘ brakes reel.
Mode slider ㉛ slides.
Brake releasing lever ㊱ starts.
Tension regulator lever ㉙ starts.
Tension regulator band ㉚ is released.
Control motor ② stops.
Plunger solenoid ⑦ turns off.
Reverse SB lever ㊸ brakes T reel brake.
Tension regulator releasing lever ㉟ starts.
S brake ㊳ & T brake ㊴ brake reel.
FR lever is locked in the centering position.


② Control motor
Ⓑ
③ Capstan
㉕ Pinchroller
㉙ Tension regulator lever
㉘ Slider lever
㉛ Mode slider
㉚ Tension regulator band

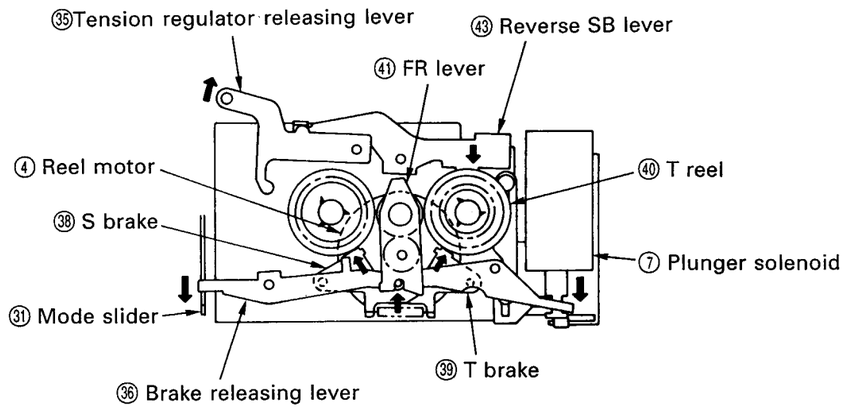
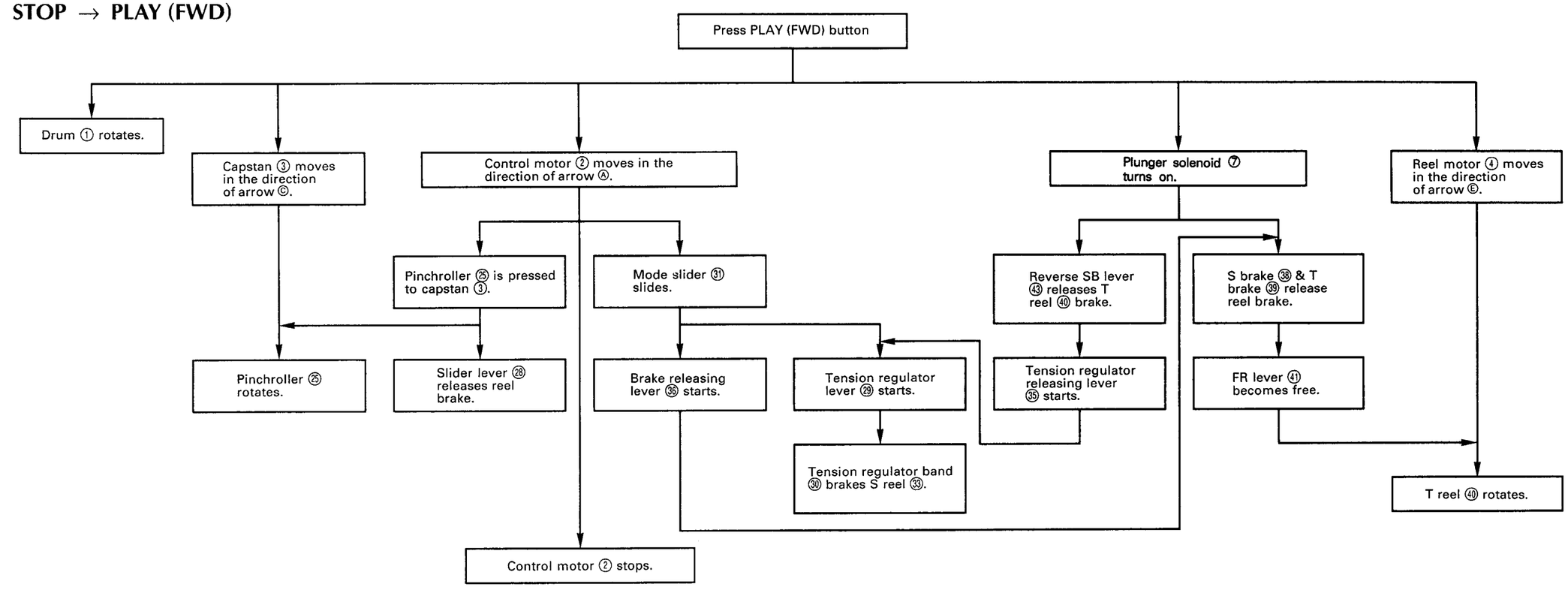
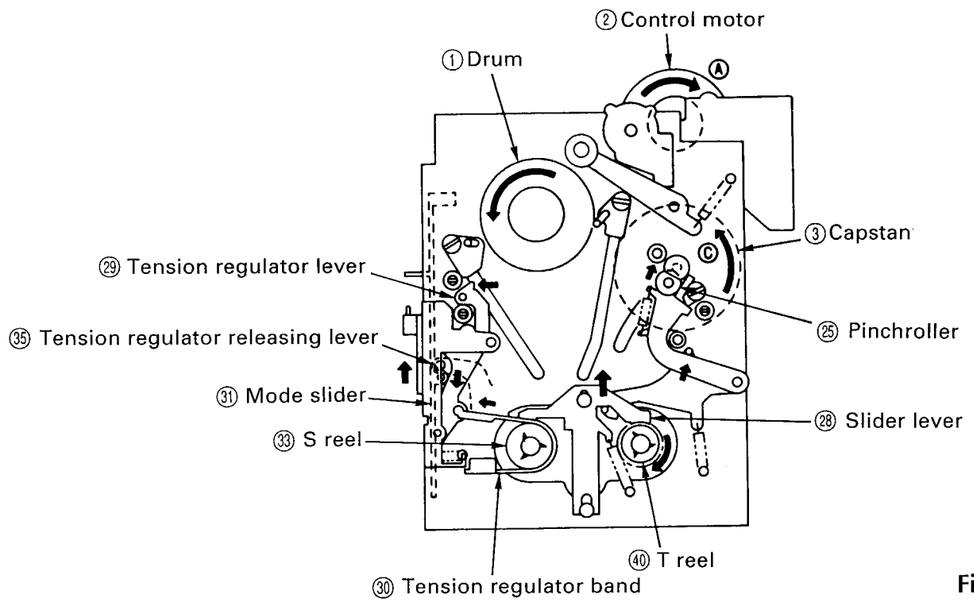

㉟Tension regulator releasing lever
㊸ Reverse SB lever
㊶ FR lever
④ Reel motor
㊵ T reel
㊳ S brake
⑦ Plunger solenoid
㉛ Mode slider
㊴ T brake
㊱ Brake releasing lever

Fig. 9-8

9-2-3 STOP → PLAY (FWD)





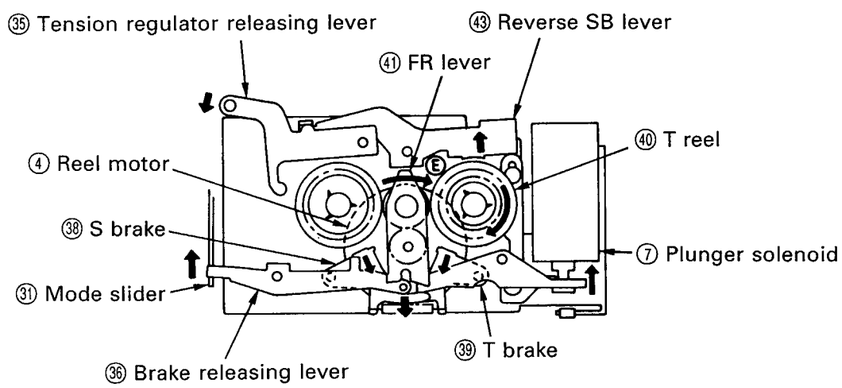
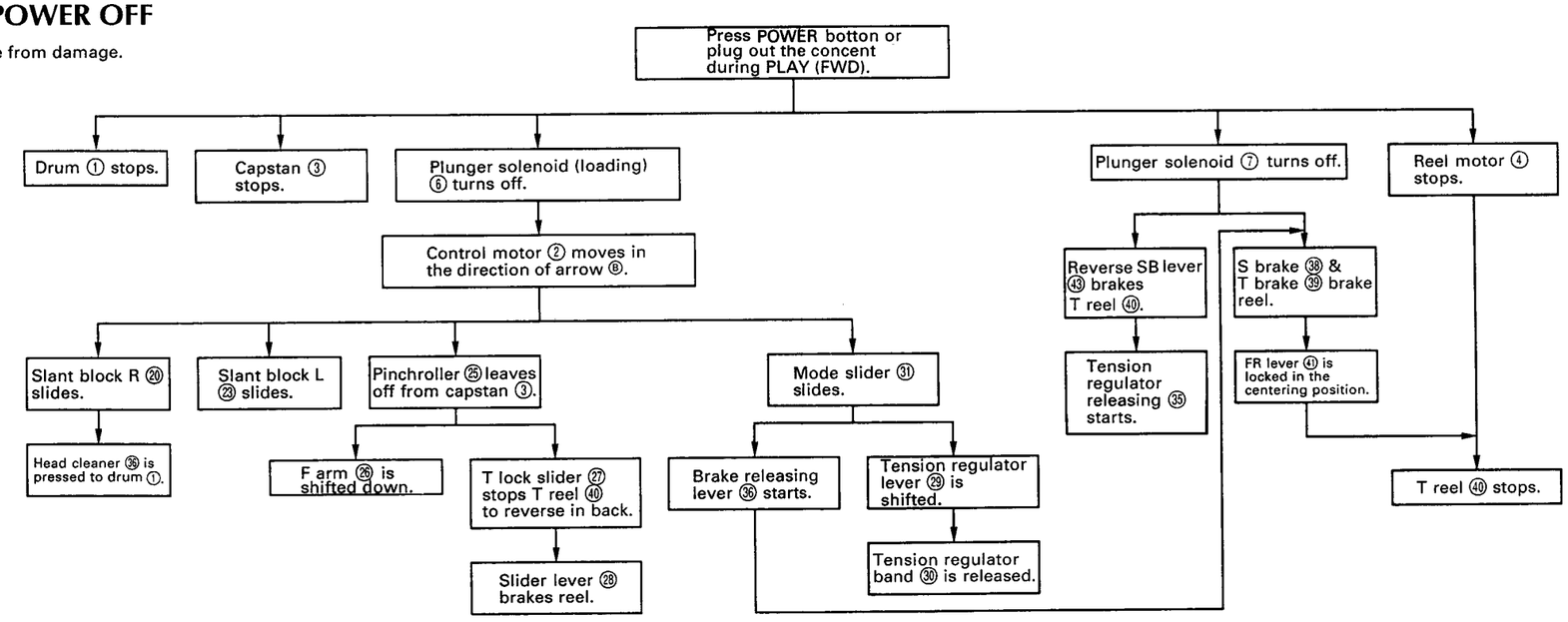
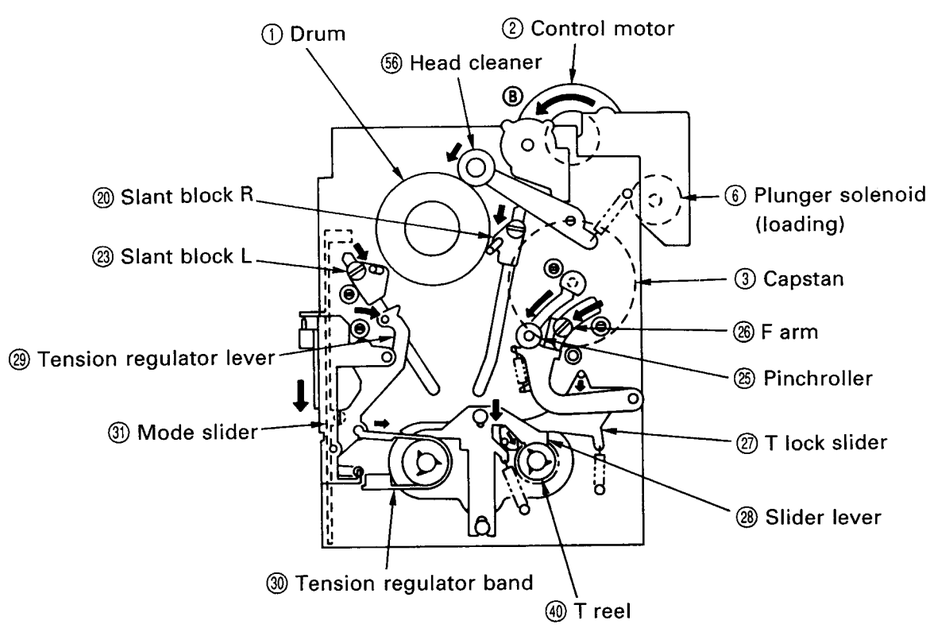


Fig. 9-9

9-2-4 PLAY (FWD) → POWER OFF

The operation is for resisting tape from damage.





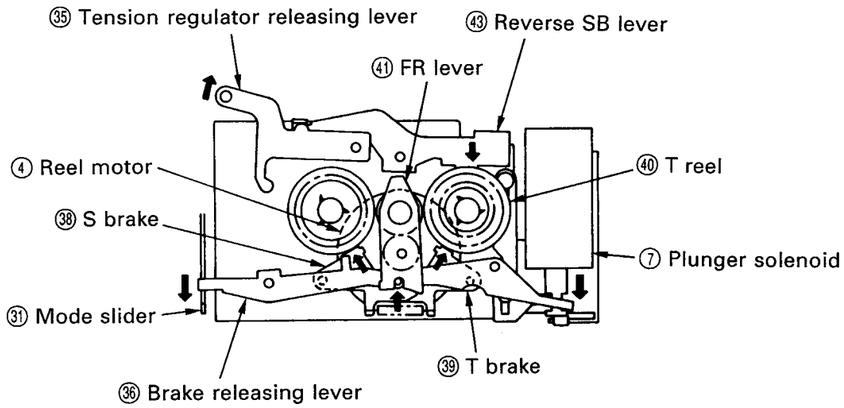
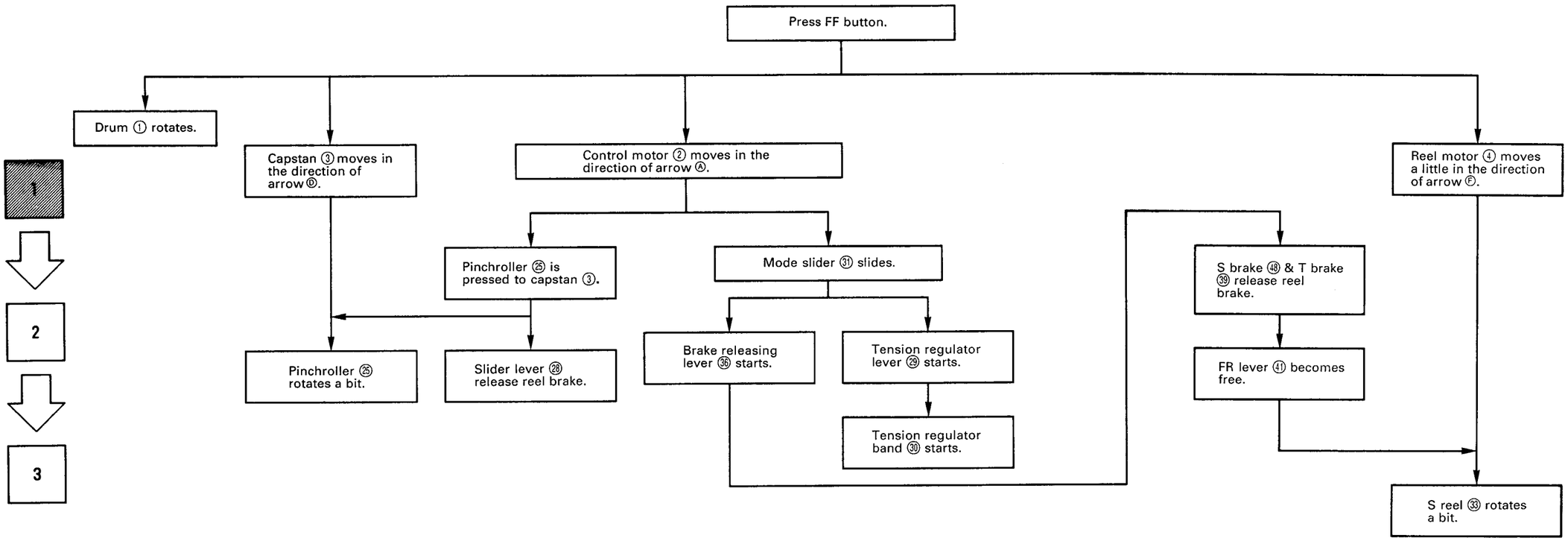
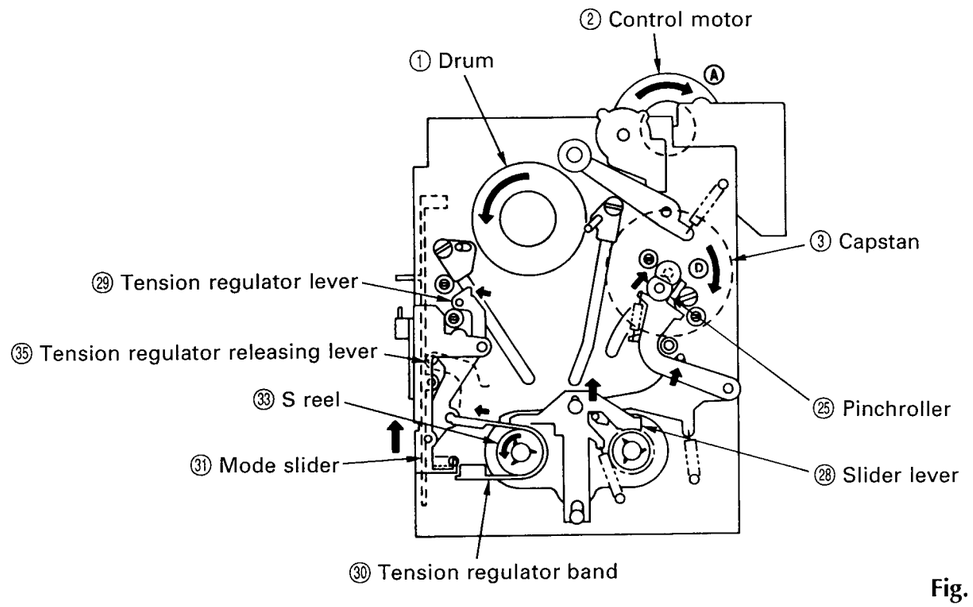


Fig. 9-10

9-2-5 STOP → FF

The operation depicts after FF more than 13 seconds.





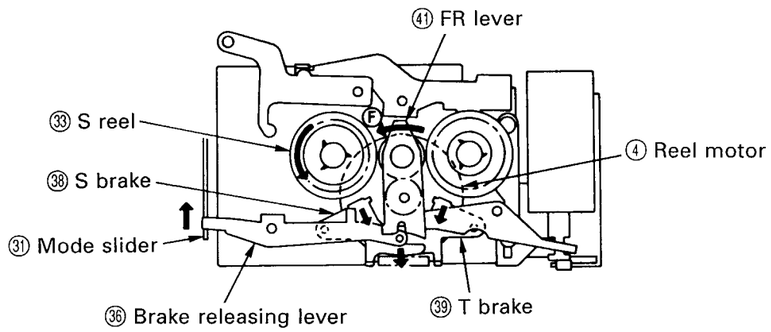
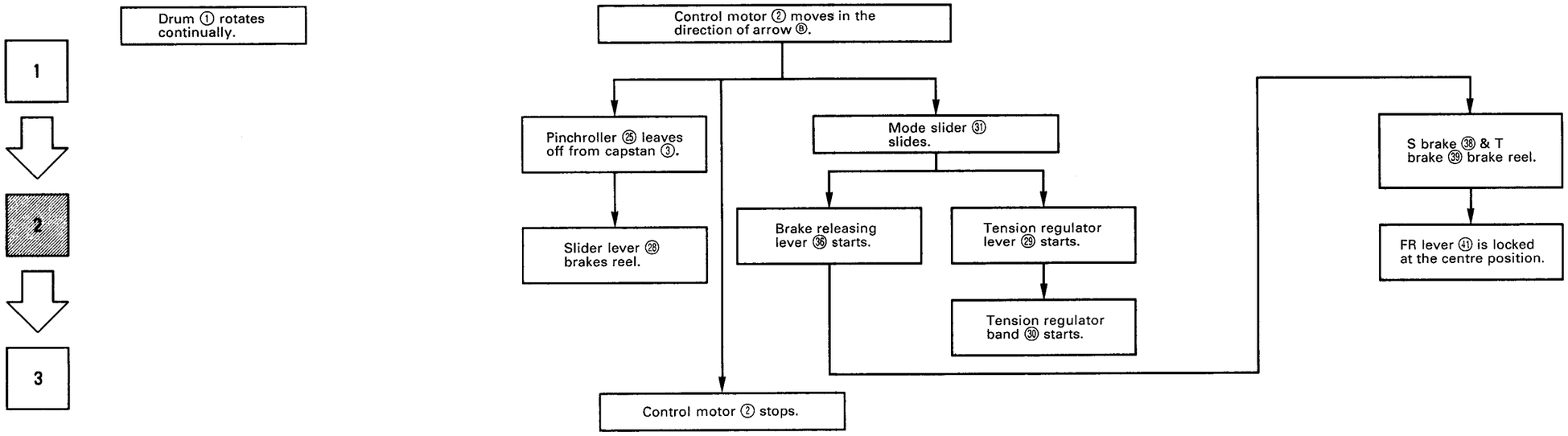
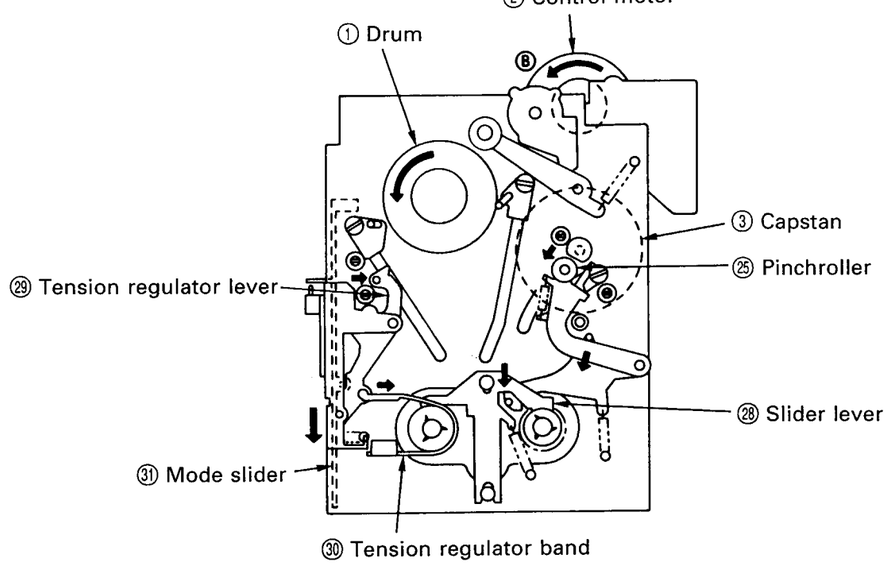


Fig. 9-11


Drum ① rotates continually.
1
2
3
Control motor ② moves in the direction of arrow Ⓑ.
Pinchroller ㉕ leaves off from capstan ③.
Slider lever ㉘ brakes reel.
Mode slider ㉛ slides.
Brake releasing lever ㊱ starts.
Tension regulator lever ㉙ starts.
Tension regulator band ㉚ starts.
S brake ㊳ & T brake ㊴ brake reel.
FR lever ㊶ is locked at the centre position.
Control motor ② stops.


② Control motor
① Drum
Ⓑ
③ Capstan
㉕ Pinchroller
㉙ Tension regulator lever
㉘ Slider lever
㉛ Mode slider
㉚ Tension regulator band

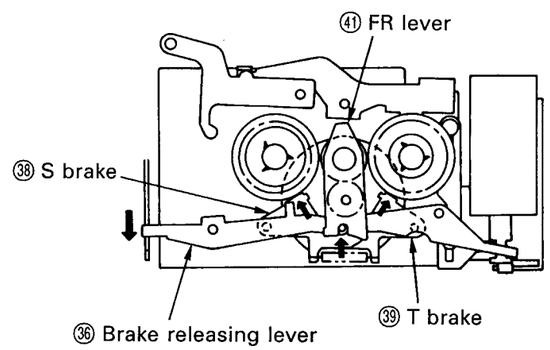
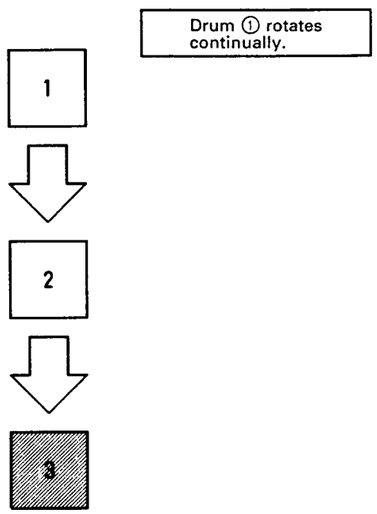
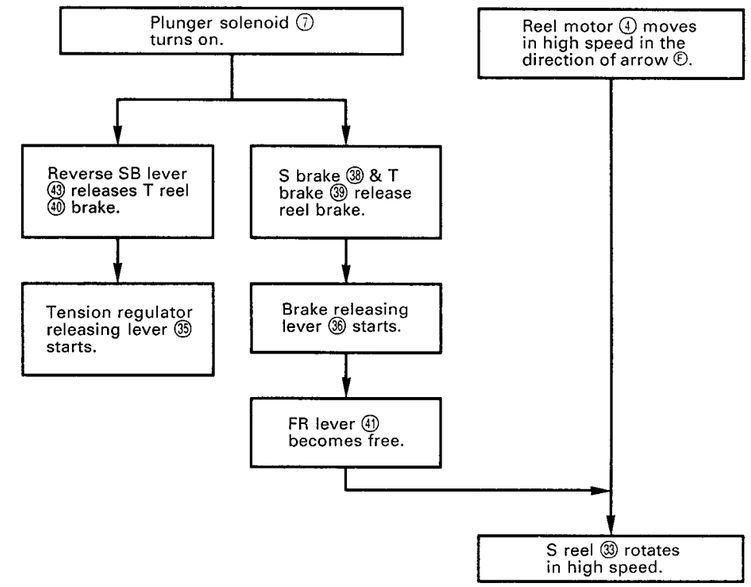
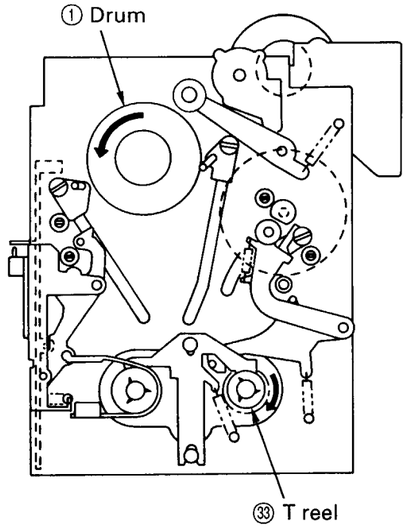

㊶ FR lever
㊳ S brake
㊱ Brake releasing lever
㊴ T brake

Fig. 9-12


Drum ① rotates continually.
1
2
3


Plunger solenoid ⑦ turns on.
Reel motor ④ moves in high speed in the direction of arrow Ⓕ.
Reverse SB lever ㊸ releases T reel ㊵ brake.
S brake ㊳ & T brake ㊴ release reel brake.
Tension regulator releasing lever ㉟ starts.
Brake releasing lever ㊱ starts.
FR lever ㊶ becomes free.
S reel ㉝ rotates in high speed.


① Drum
㉝ T reel

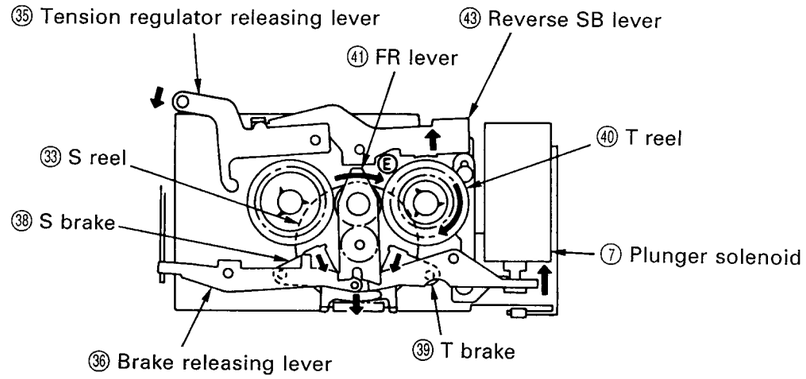
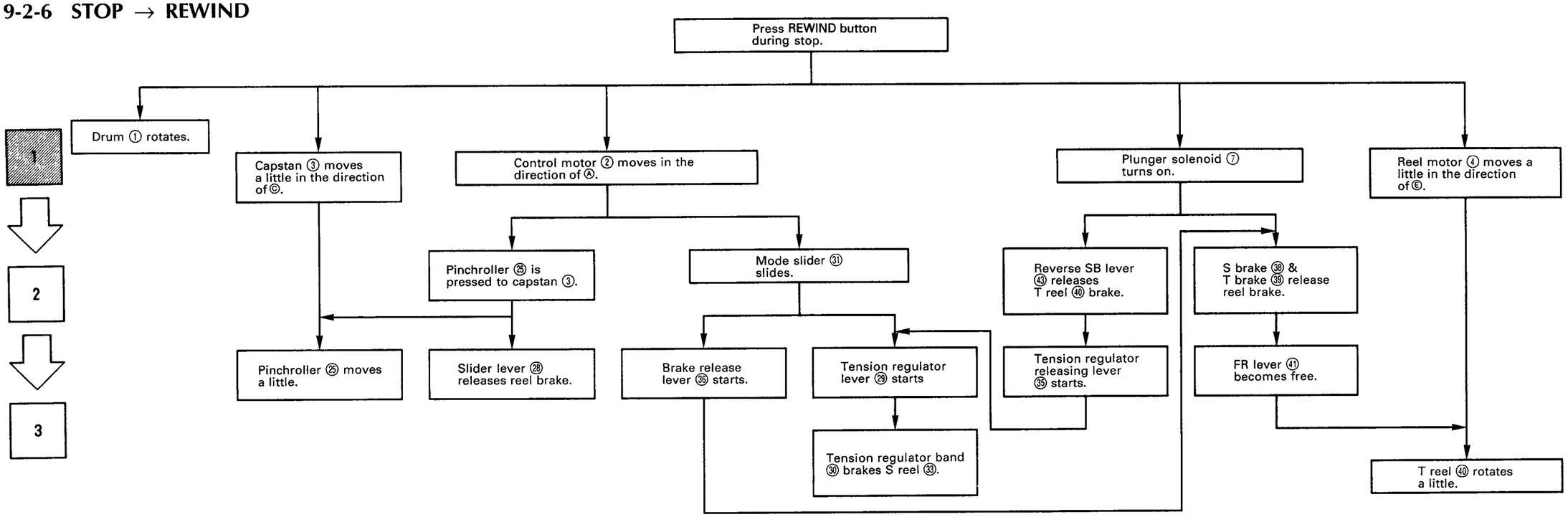
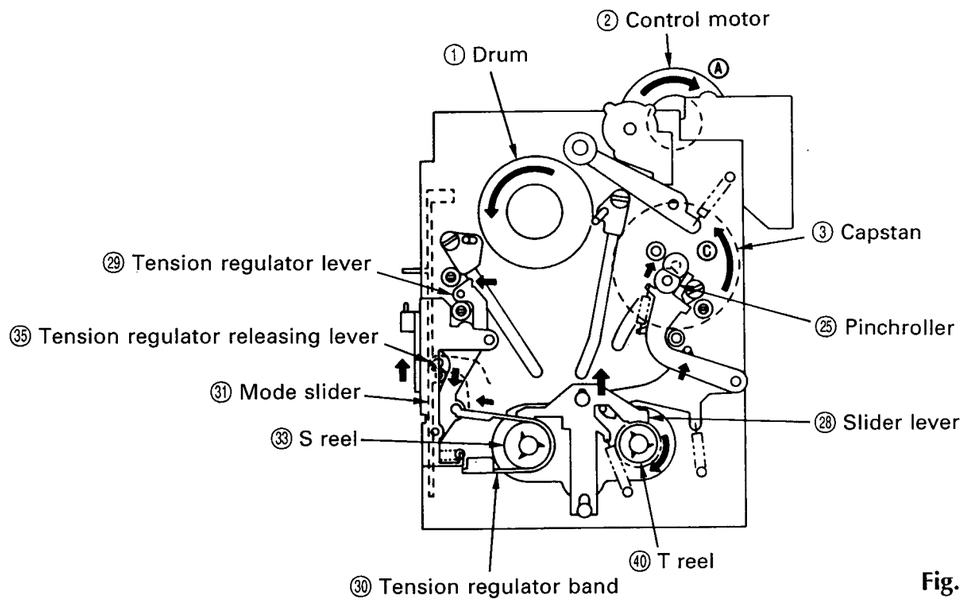

㉟ Tension regulator releasing lever
㊸ Reverse SB lever
㊶ FR lever
㊵ T reel
㉝ S reel
㊳ S brake
⑦ Plunger solenoid
㊱ Brake releasing lever
㊴ T brake

Fig. 9-13

9-2-6 STOP → REWIND





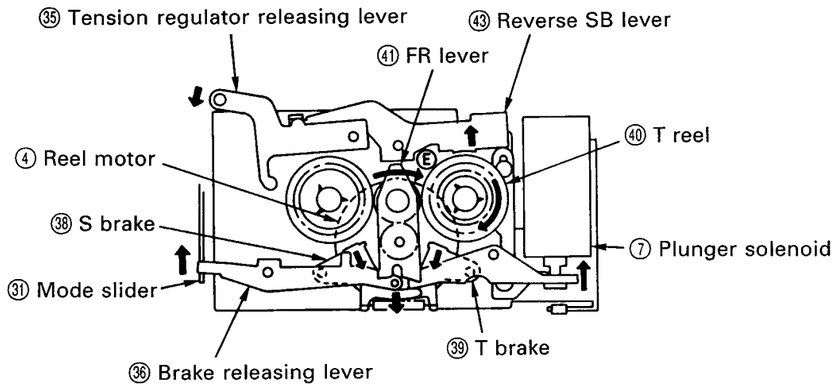
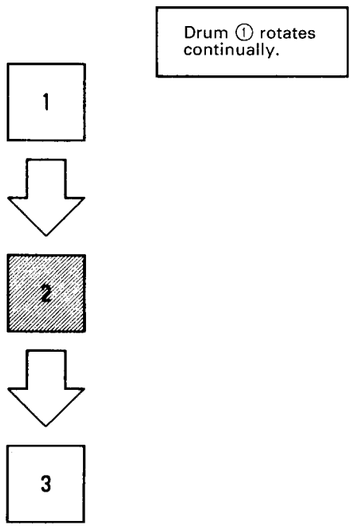
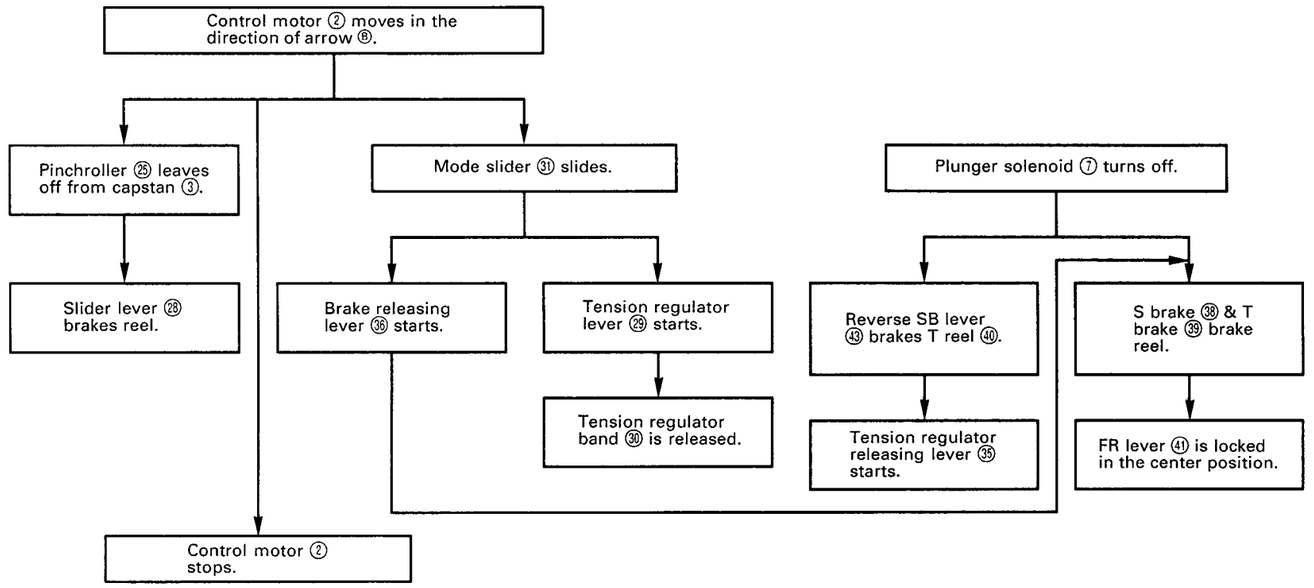


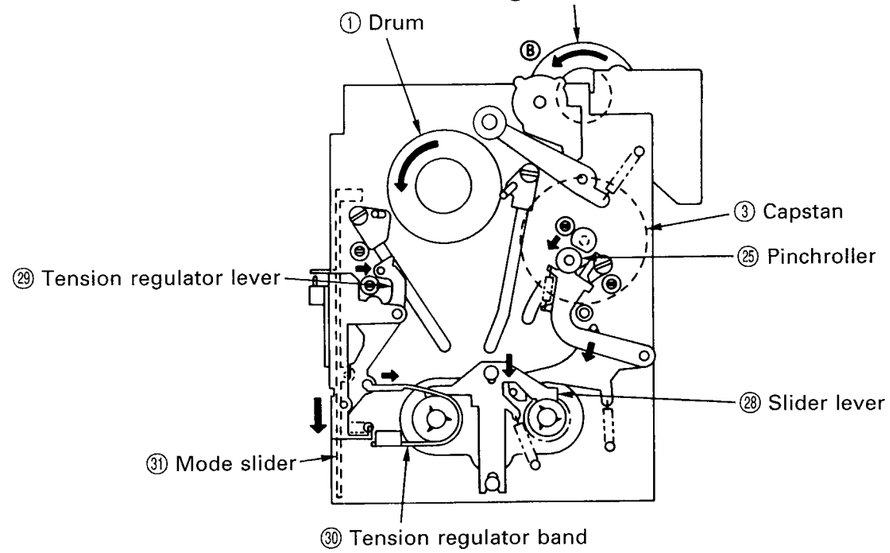
Fig. 9-14



Drum ① rotates continually.



② Control motor



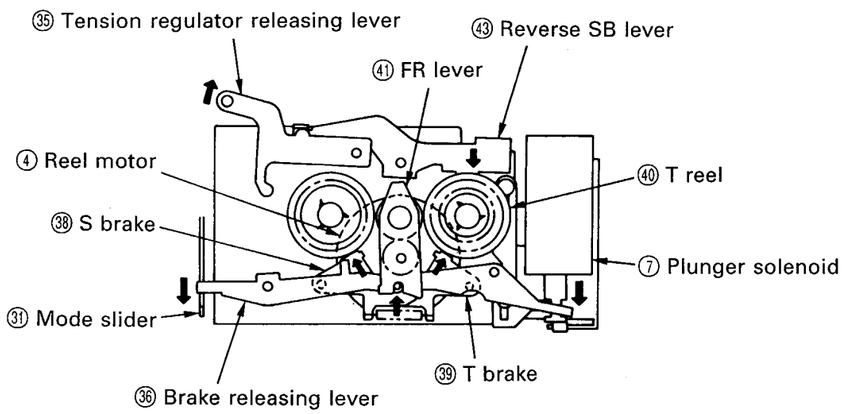
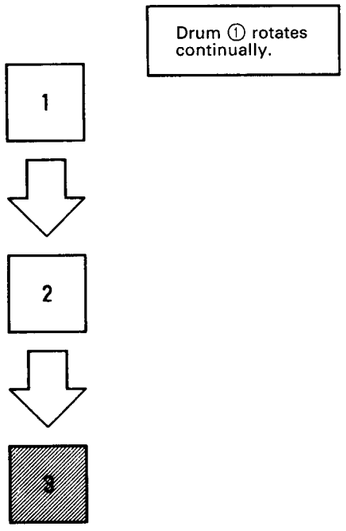
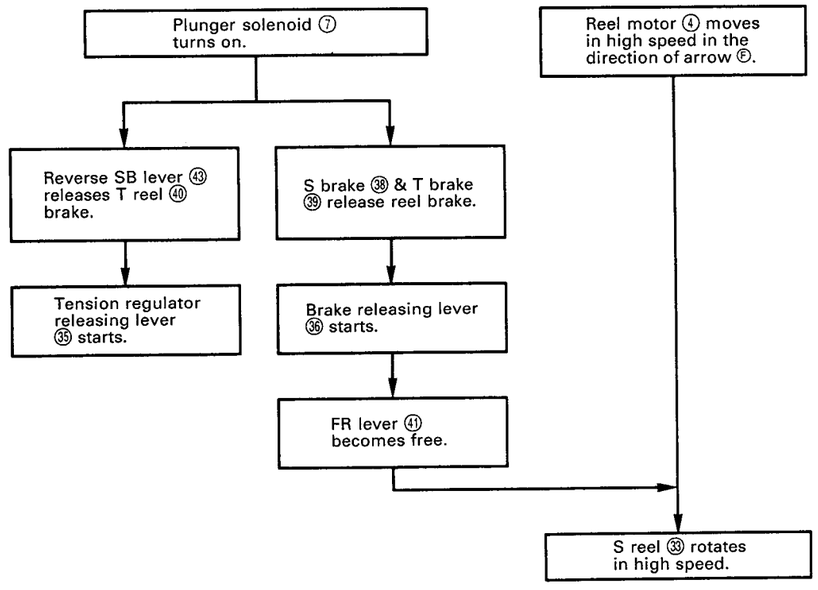
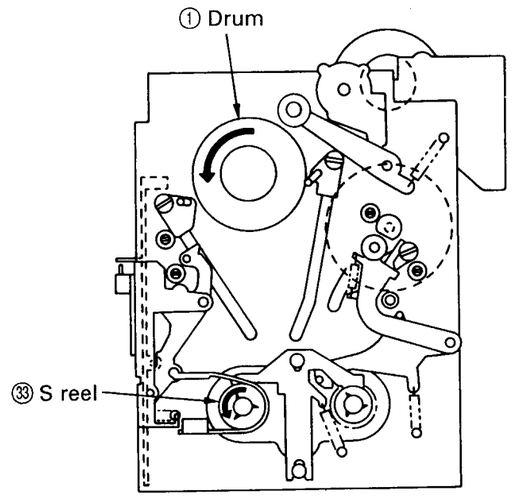


Fig. 9-15


Drum ① rotates continually.
1
2
3


Plunger solenoid ⑦ turns on.
Reel motor ④ moves in high speed in the direction of arrow Ⓕ.
Reverse SB lever ㊸ releases T reel ㊵ brake.
S brake ㊳ & T brake ㊴ release reel brake.
Tension regulator releasing lever ㉟ starts.
Brake releasing lever ㊱ starts.
FR lever ㊶ becomes free.
S reel ㉝ rotates in high speed.


① Drum
㉝ S reel

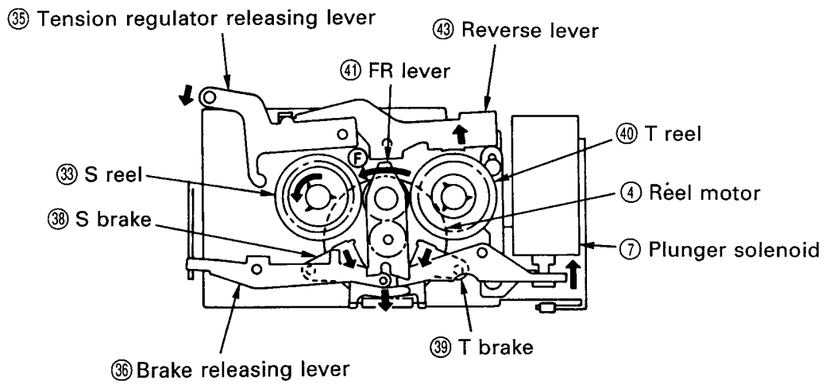
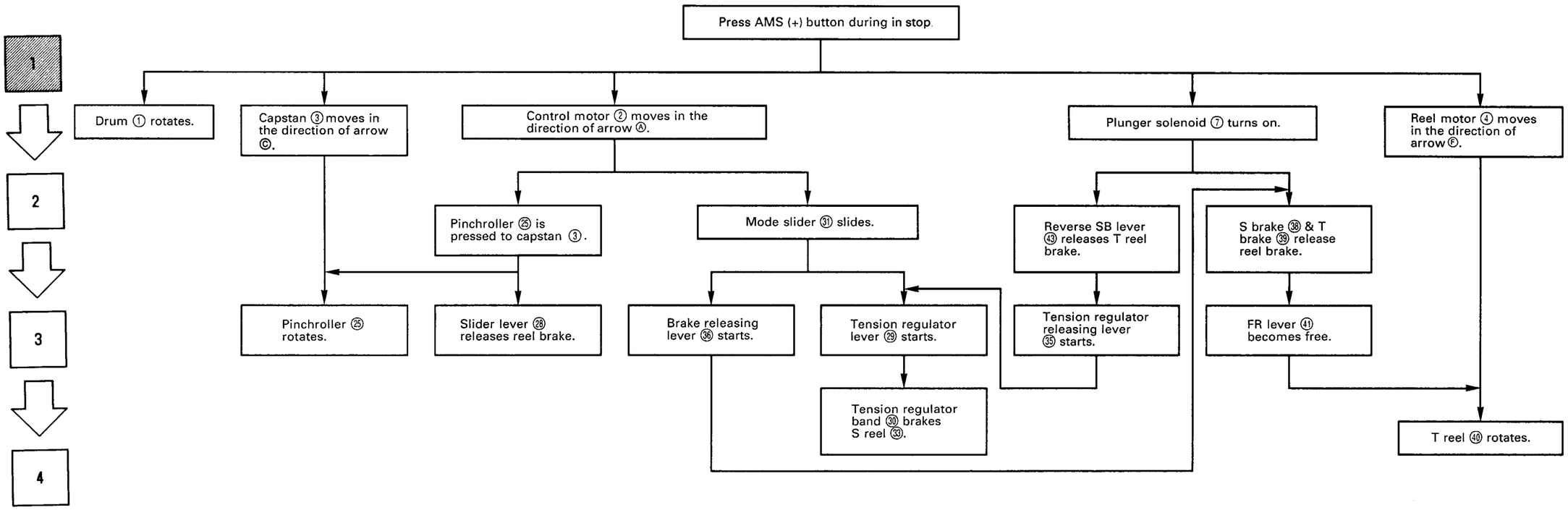
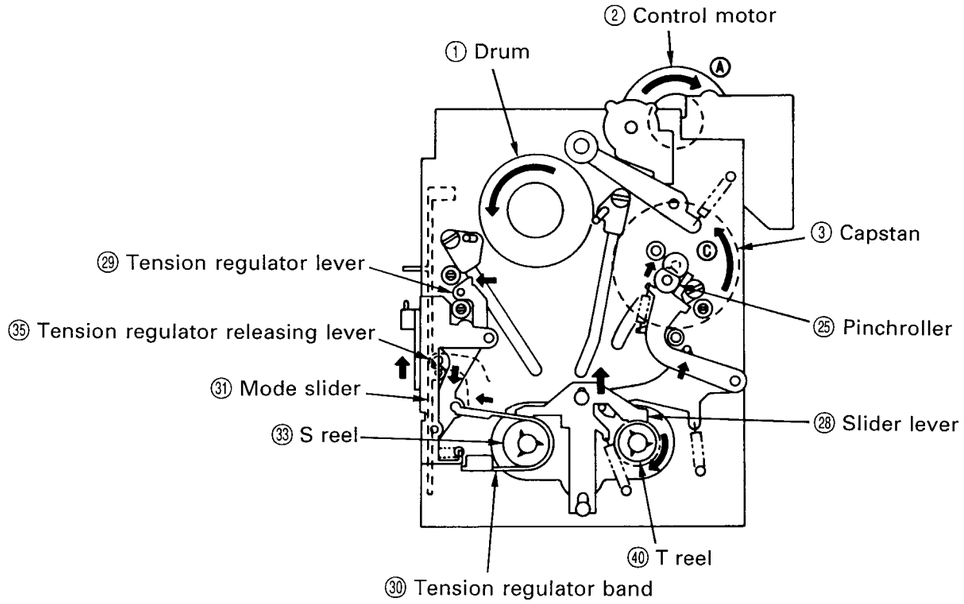

㉟ Tension regulator releasing lever
㊸ Reverse lever
㊶ FR lever
㊵ T reel
㉝ S reel
④ Reel motor
㊳ S brake
⑦ Plunger solenoid
㊴ T brake
㊱ Brake releasing lever

Fig. 9-16

9-2-7 STOP → AMS (+) 1/2





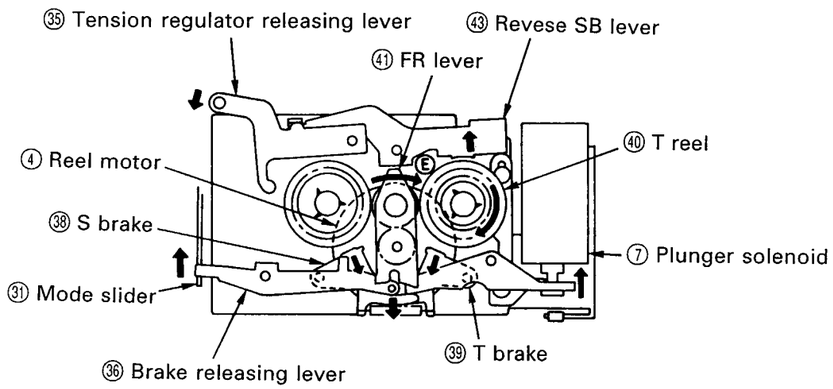
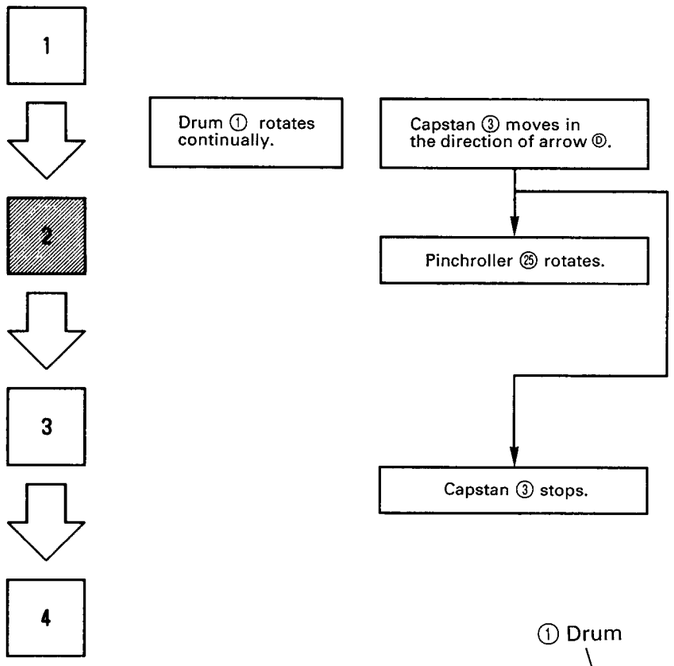
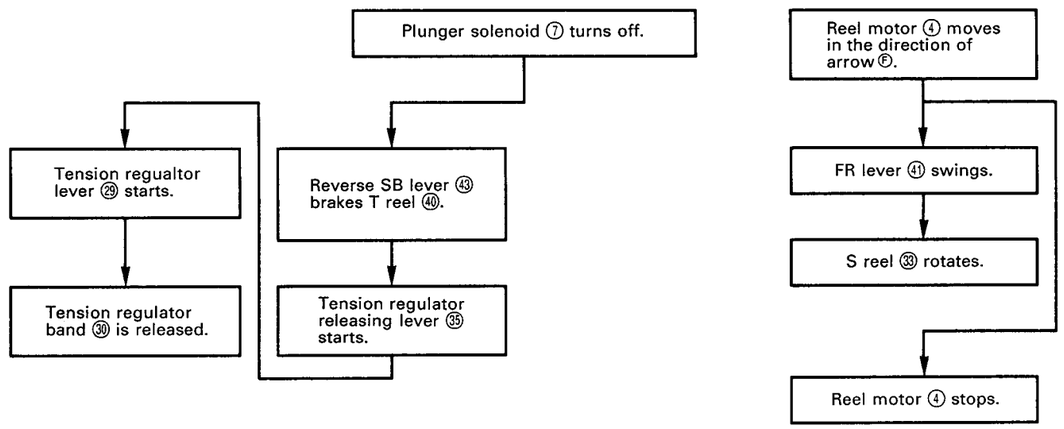
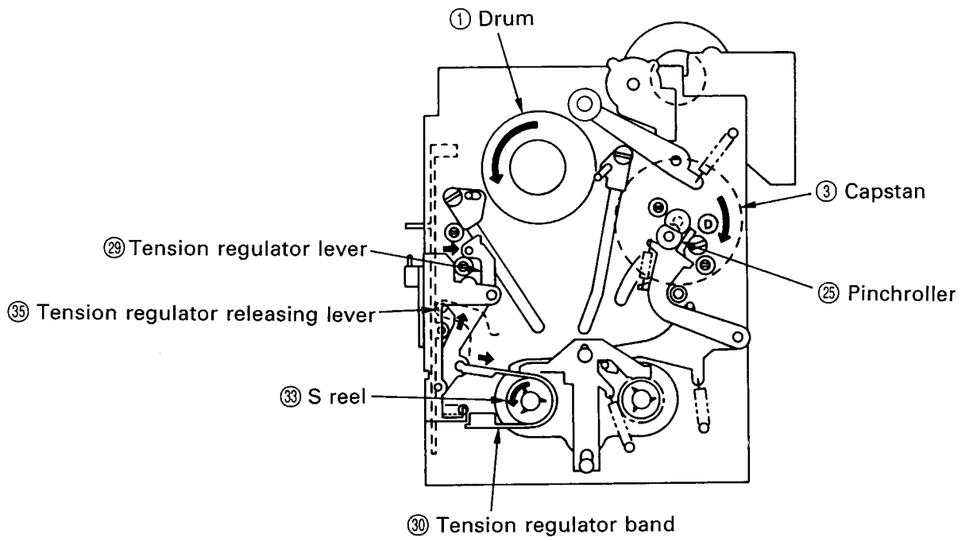


Fig. 9-17


1
Drum ① rotates continually.
Capstan ③ moves in the direction of arrow Ⓓ.
2
Pinchroller ㉕ rotates.
3
Capstan ③ stops.
4


Plunger solenoid ⑦ turns off.
Tension regualtor lever ㉙ starts.
Reverse SB lever ㊸ brakes T reel ㊵.
Tension regulator band ㉚ is released.
Tension regulator releasing lever ㉟ starts.
Reel motor ④ moves in the direction of arrow Ⓕ.
FR lever ㊶ swings.
S reel ㉝ rotates.
Reel motor ④ stops.


① Drum
③ Capstan
㉙ Tension regulator lever
㉕ Pinchroller
㉟ Tension regulator releasing lever
㉝ S reel
㉚ Tension regulator band

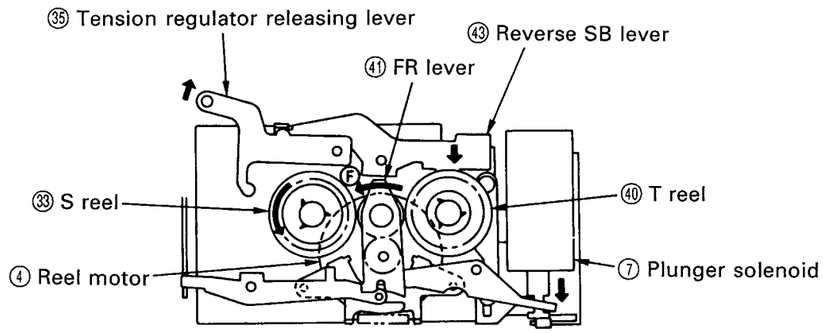
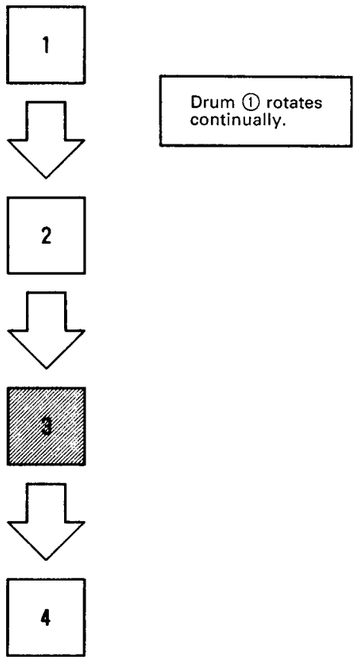
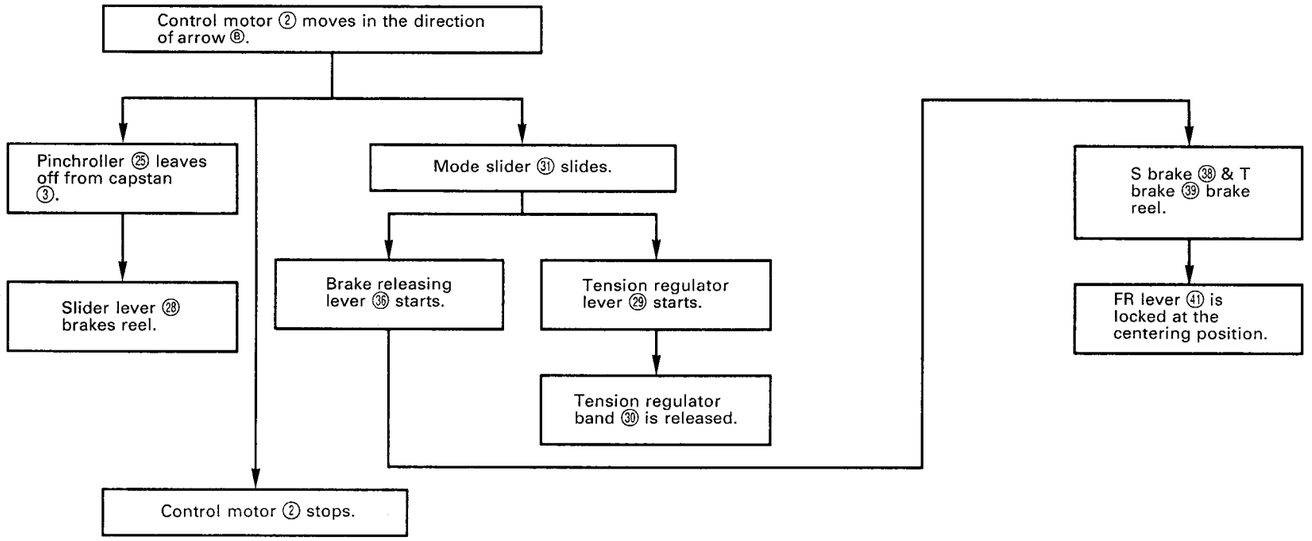

㉟ Tension regulator releasing lever
㊸ Reverse SB lever
㊶ FR lever
㉝ S reel
㊵ T reel
④ Reel motor
⑦ Plunger solenoid

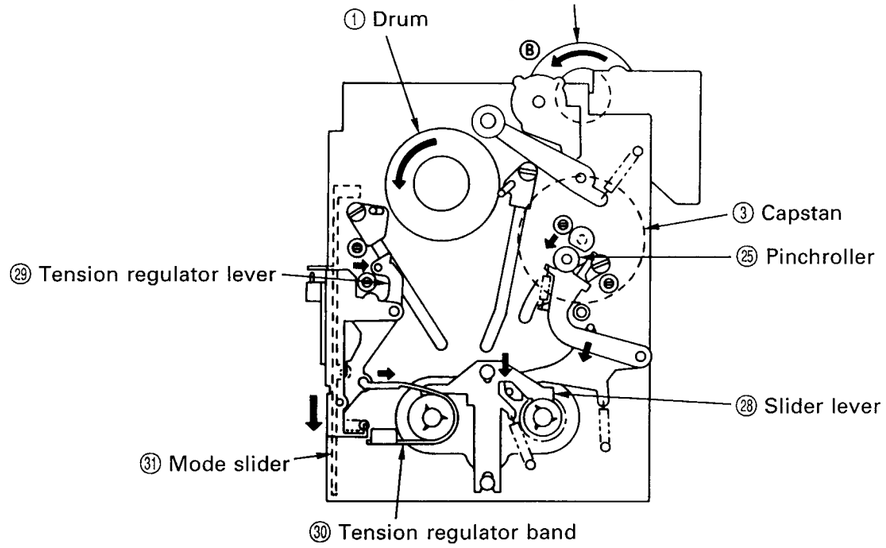
Fig. 9-18



Drum ① rotates continually.



② Control motor



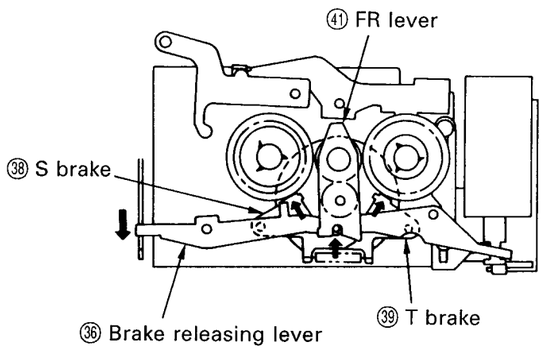
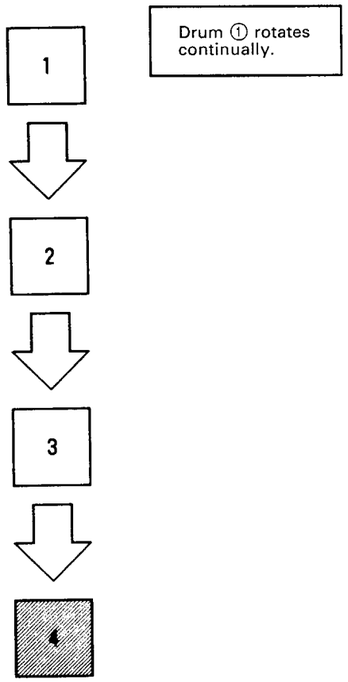
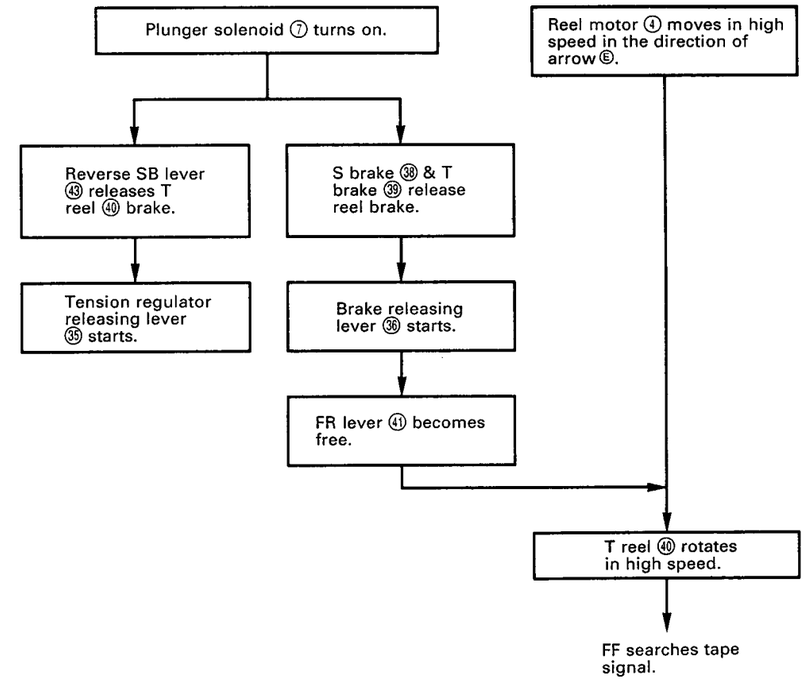
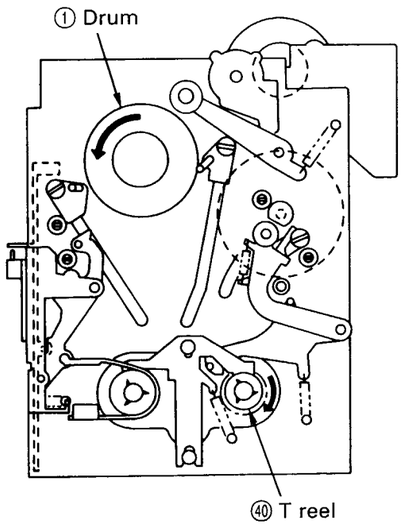


Fig. 9-19



Drum ① rotates continually.





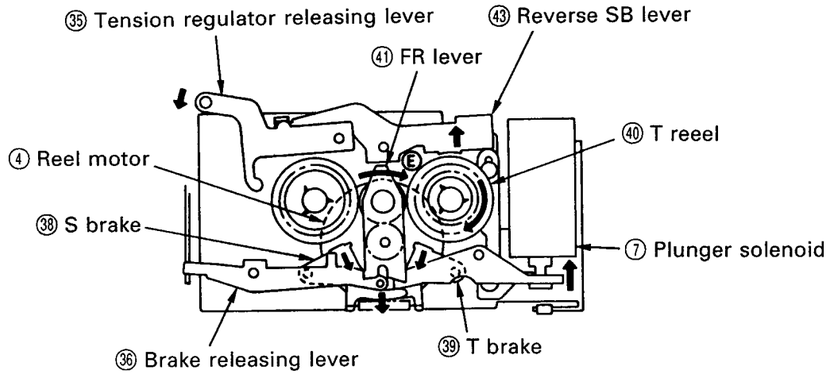
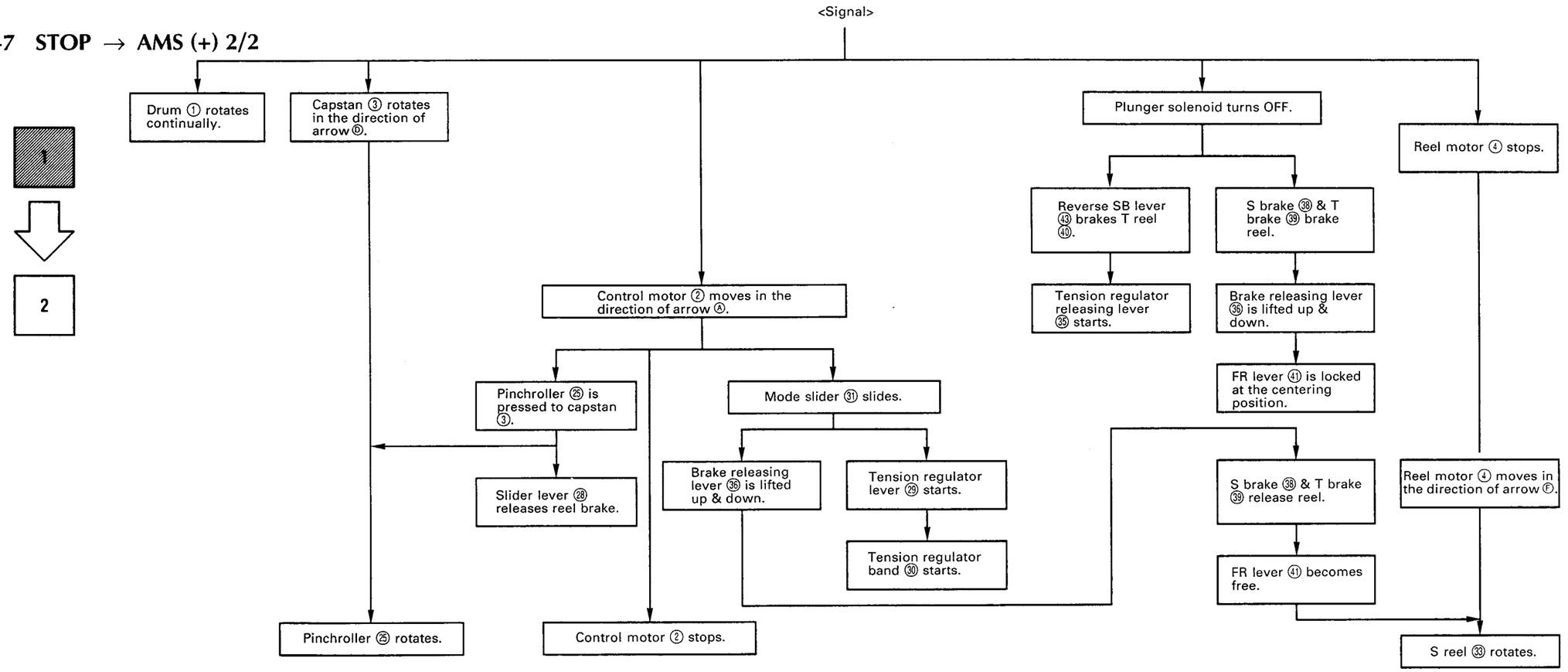
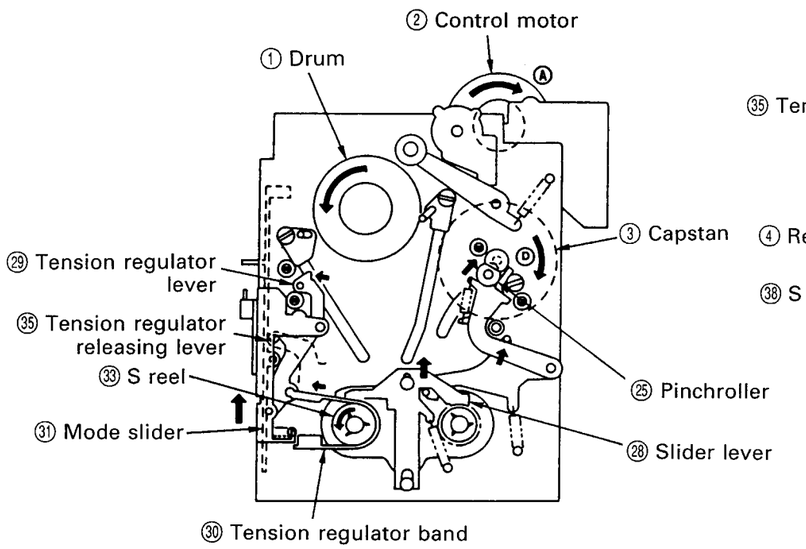
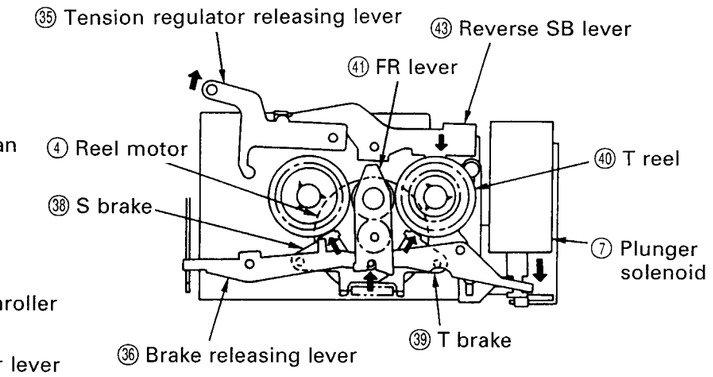


Fig. 9-20

9-2-7 STOP → AMS (+) 2/2







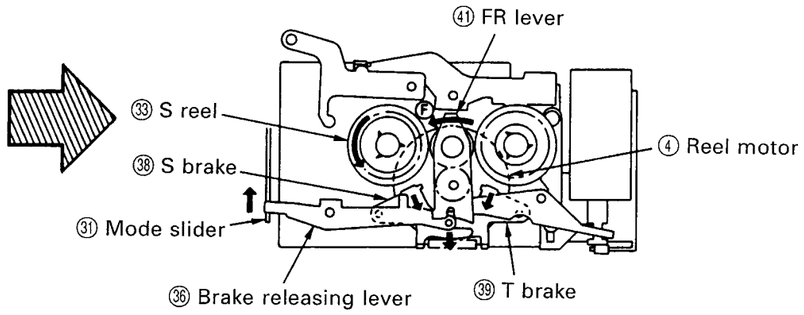
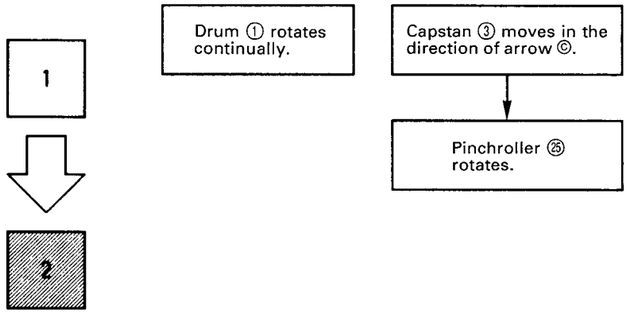
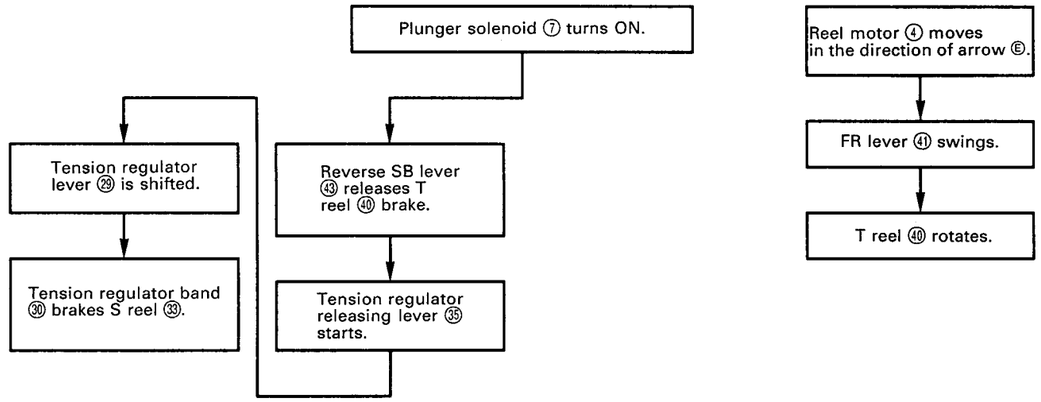
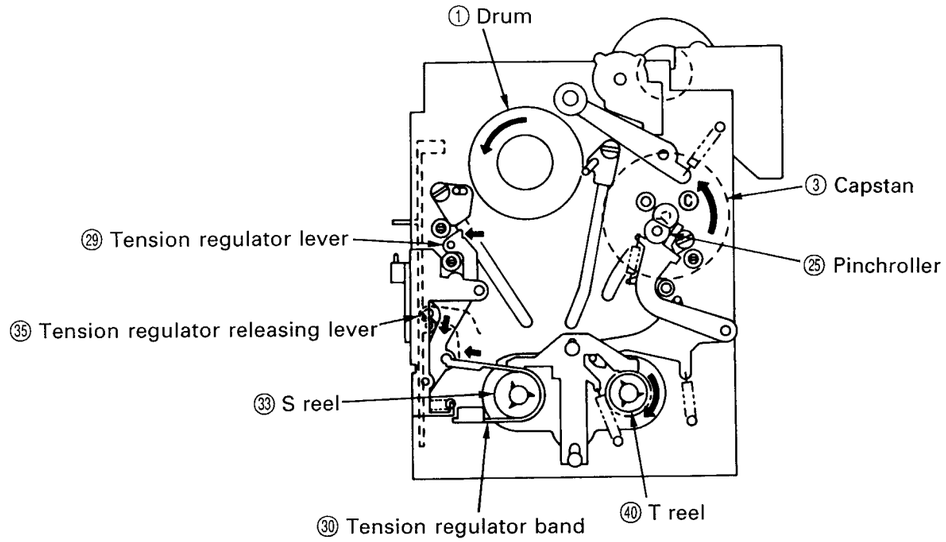


Fig. 9-21


1
2
Drum ① rotates continually.
Capstan ③ moves in the direction of arrow Ⓒ.
Pinchroller ㉕ rotates.


Plunger solenoid ⑦ turns ON.
Tension regulator lever ㉙ is shifted.
Tension regulator band ㉚ brakes S reel ㉝.
Reverse SB lever ㊸ releases T reel ㊵ brake.
Tension regulator releasing lever ㉟ starts.
Reel motor ④ moves in the direction of arrow Ⓔ.
FR lever ㊶ swings.
T reel ㊵ rotates.


① Drum
③ Capstan
㉙ Tension regulator lever
㉕ Pinchroller
㉟ Tension regulator releasing lever
㉝ S reel
㉚ Tension regulator band
㊵ T reel

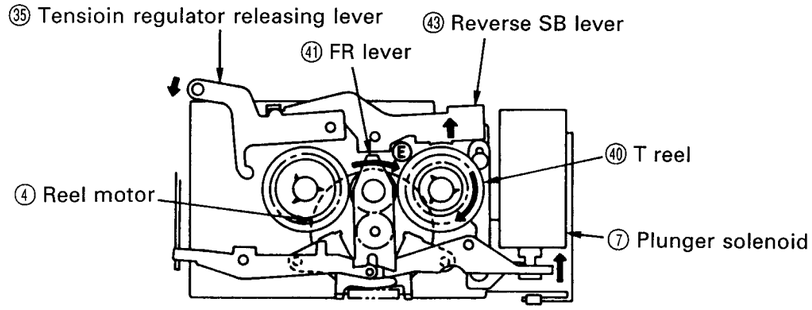
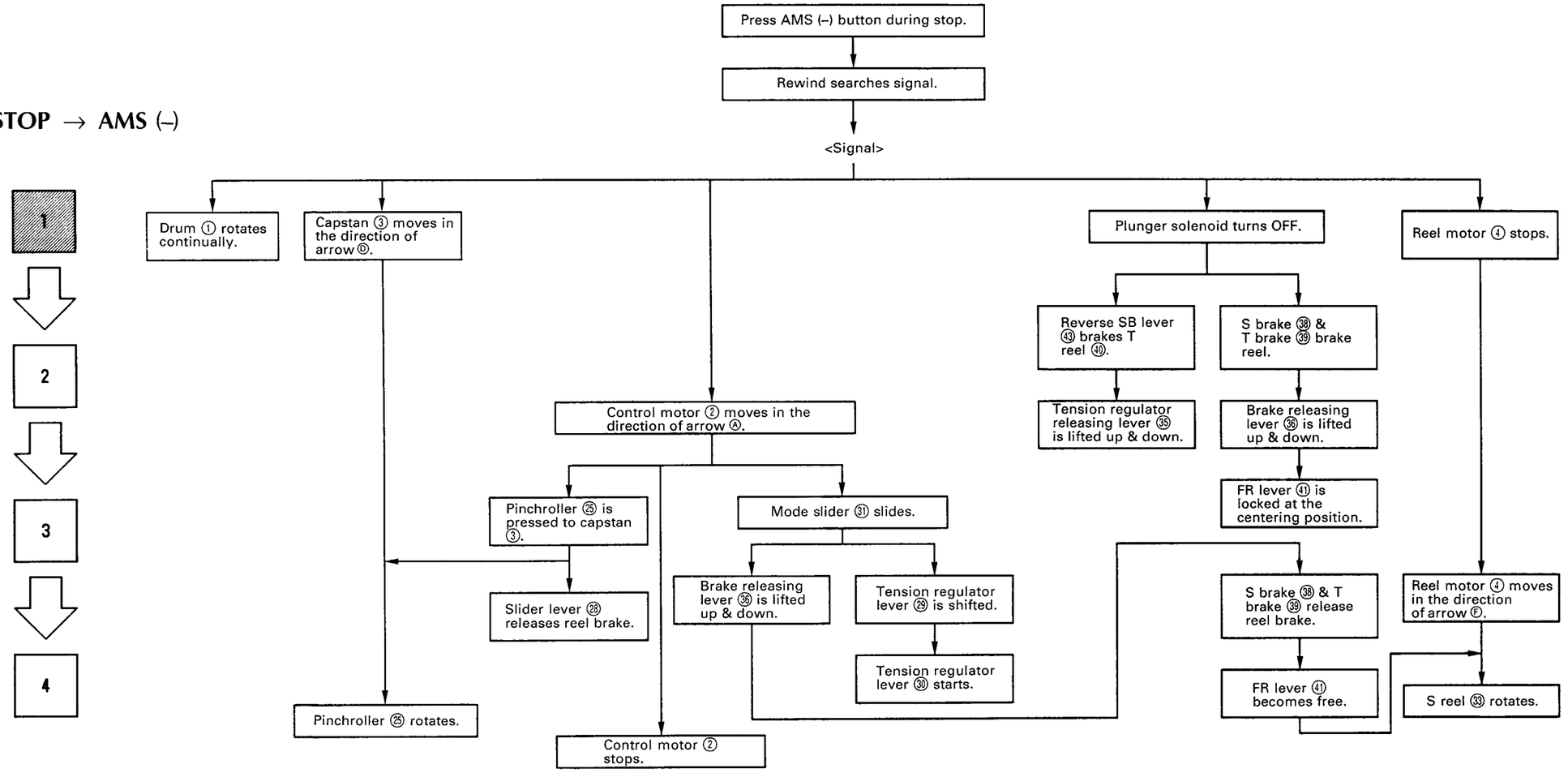

㉟ Tensioin regulator releasing lever
㊸ Reverse SB lever
㊶ FR lever
㊵ T reel
④ Reel motor
⑦ Plunger solenoid

Fig. 9-22

9-2-8 STOP → AMS (–)



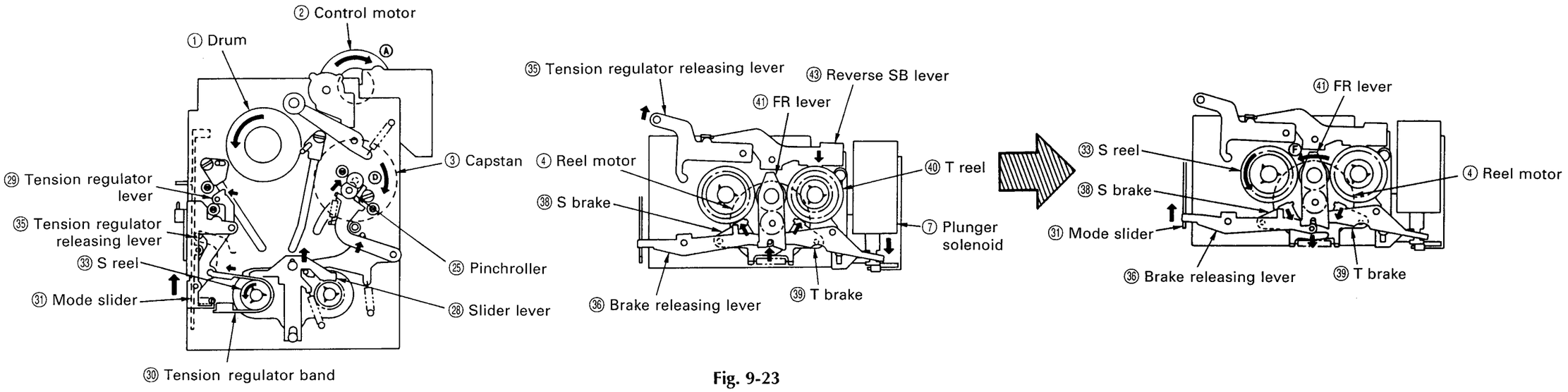


Fig. 9-23

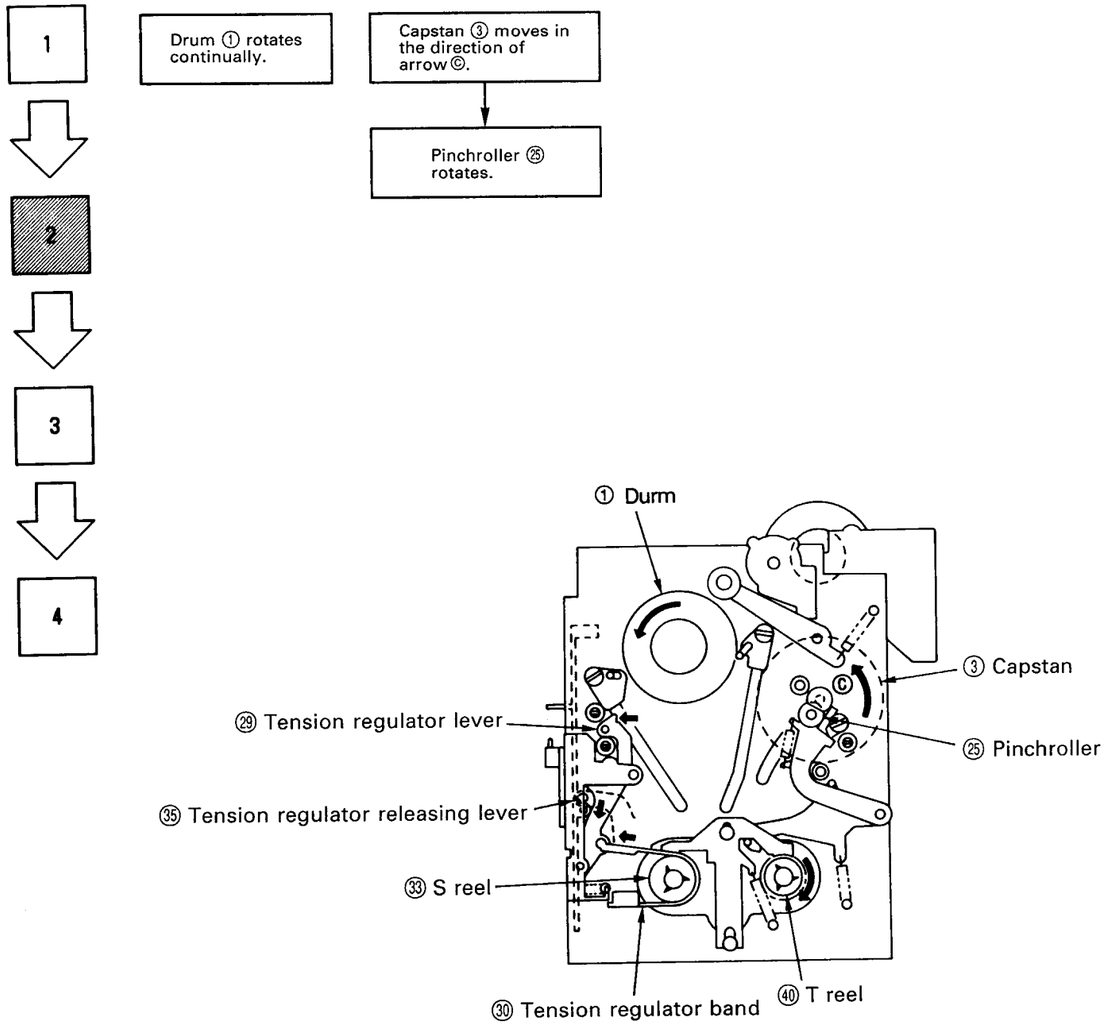

1
Drum ① rotates continually.
Capstan ③ moves in the direction of arrow Ⓒ.
Pinchroller ㉕ rotates.
2
3
4
Plunger solenoid ⑦ turns ON.
Tension regulator lever ㉙ is shifted.
Tension regulator band ㉚ brakes S reel.
Reverse SB lever ㊸ releases T reel ㊵ brake.
Tension regulator releasing lever ㉟ is lifted down.
Reel motor ④ moves in the direction of arrow Ⓔ.
FR lever ㊶ swings.
T reel ㊵ rotates.
① Durm
③ Capstan
㉙ Tension regulator lever
㉕ Pinchroller
㉟ Tension regulator releasing lever
㉝ S reel
㉚ Tension regulator band
㊵ T reel
㉟ Tension regulator lever
㊸ Reverse SB lever
㊶ FR lever
㉝ S reel
㊵ T reel
④ Reel motor
⑦ Plunger solenoid

Fig. 9-24

1

2

3

4

Drum ① rotates continually.

Capstan ③ moves in the direction of arrow Ⓓ.

Pinchroller ㉕ rotates.

Plunger solenoid ⑦ turns OFF.

Tension regulator lever ㉙ starts.

Tension regulator band ㉚ is released.

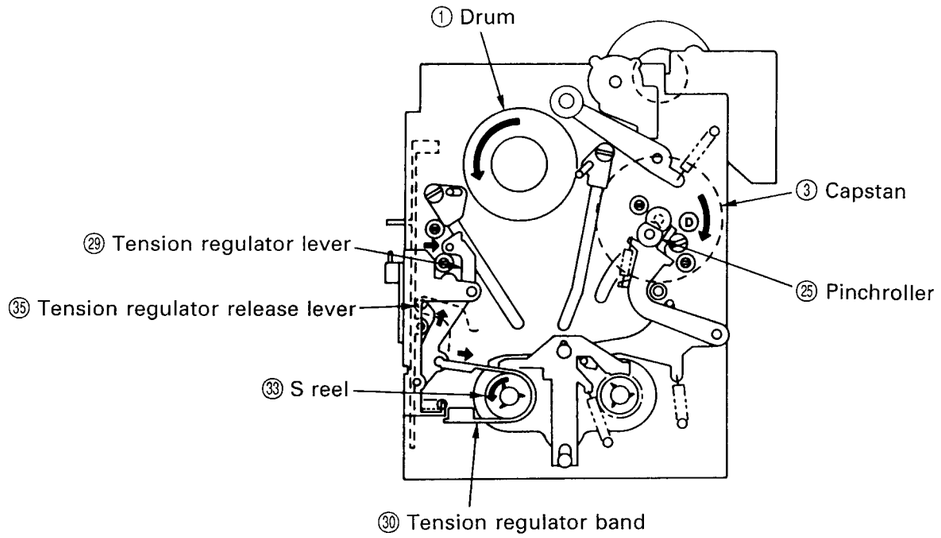
Reverse SB lever ㊸ brakes T reel ㊵.

Tension regulator releasing lever ㉟ is lifted up.

Reel motor ④ moves in the direction of arrow Ⓕ.

FR lever ㊶ swngs.

T reel ㊵ rotates.



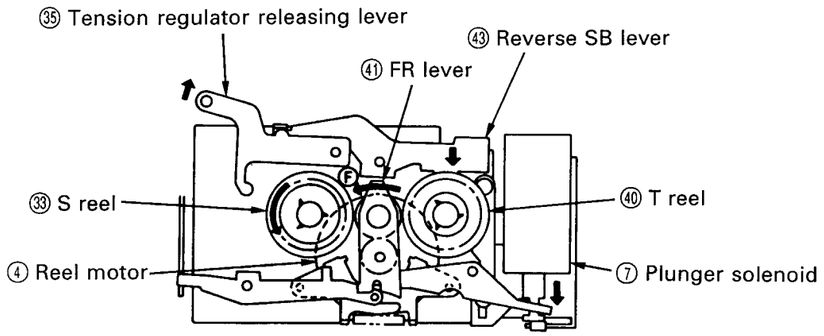


Fig. 9-25

1

Drum ① rotates continually.

Capstan ③ moves in the direction of arrow ©.

Pinchroller ㉕ rotates.

2

Plunger solenoid ⑦ turns ON.

Tension regulator lever ㉙ starts.

Tension regulator band ㉚ brakes S reel ㉝.

Reverse SB lever ㊸ releases T reel brake.

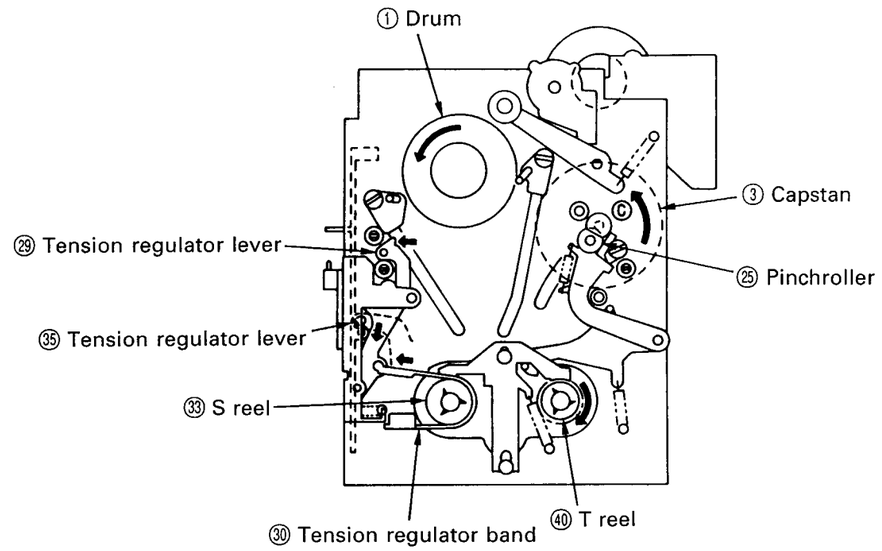
Tension regulator releasing lever ㉟ is shifted down.

3

Reel motor ④ moves in the direction of arrow Ⓔ.

FR lever ㊶ swngs.

T reel ㉝ rotates.



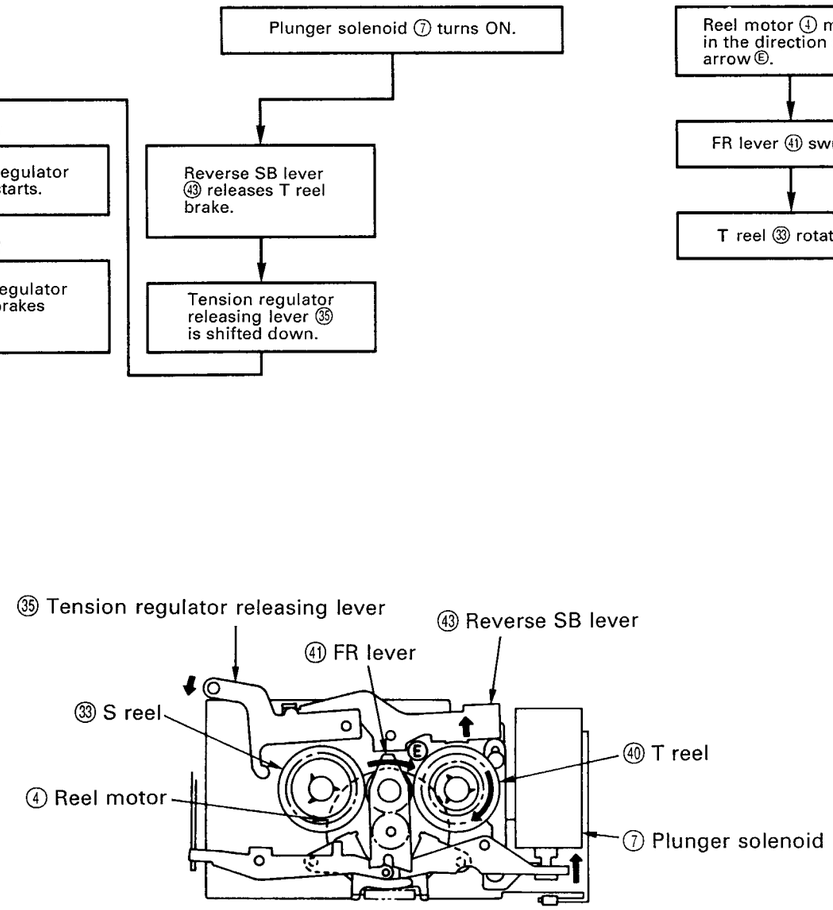
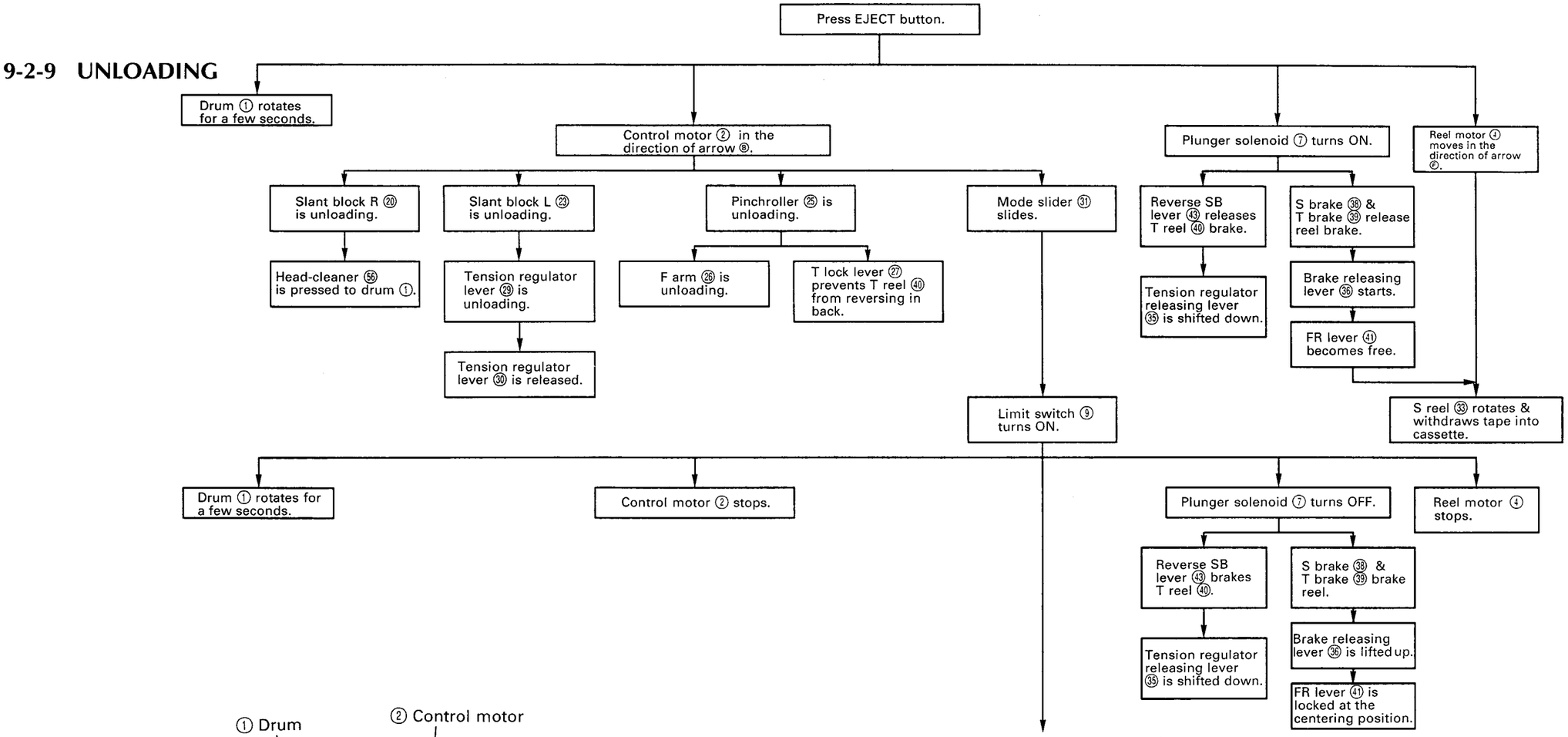
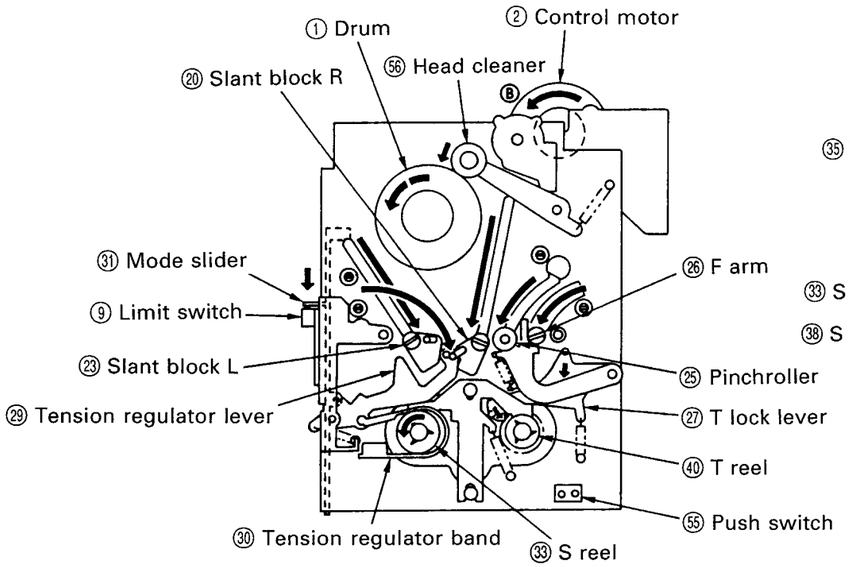
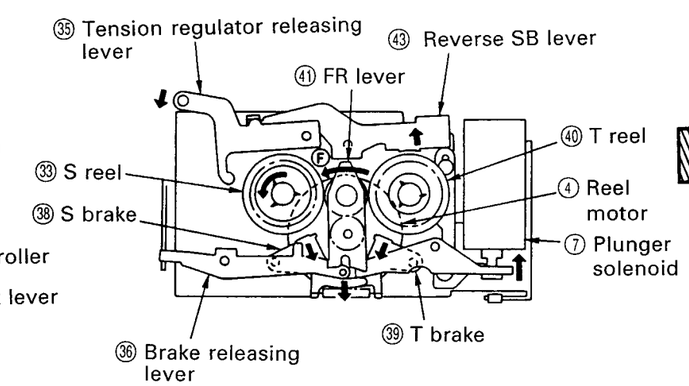


Fig. 9-26

9-2-9 UNLOADING







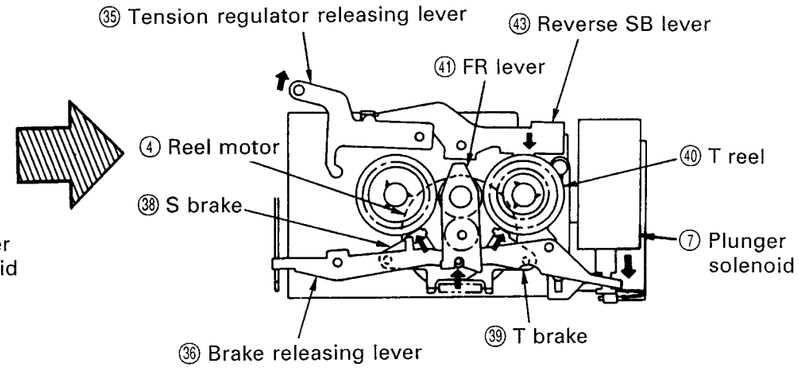
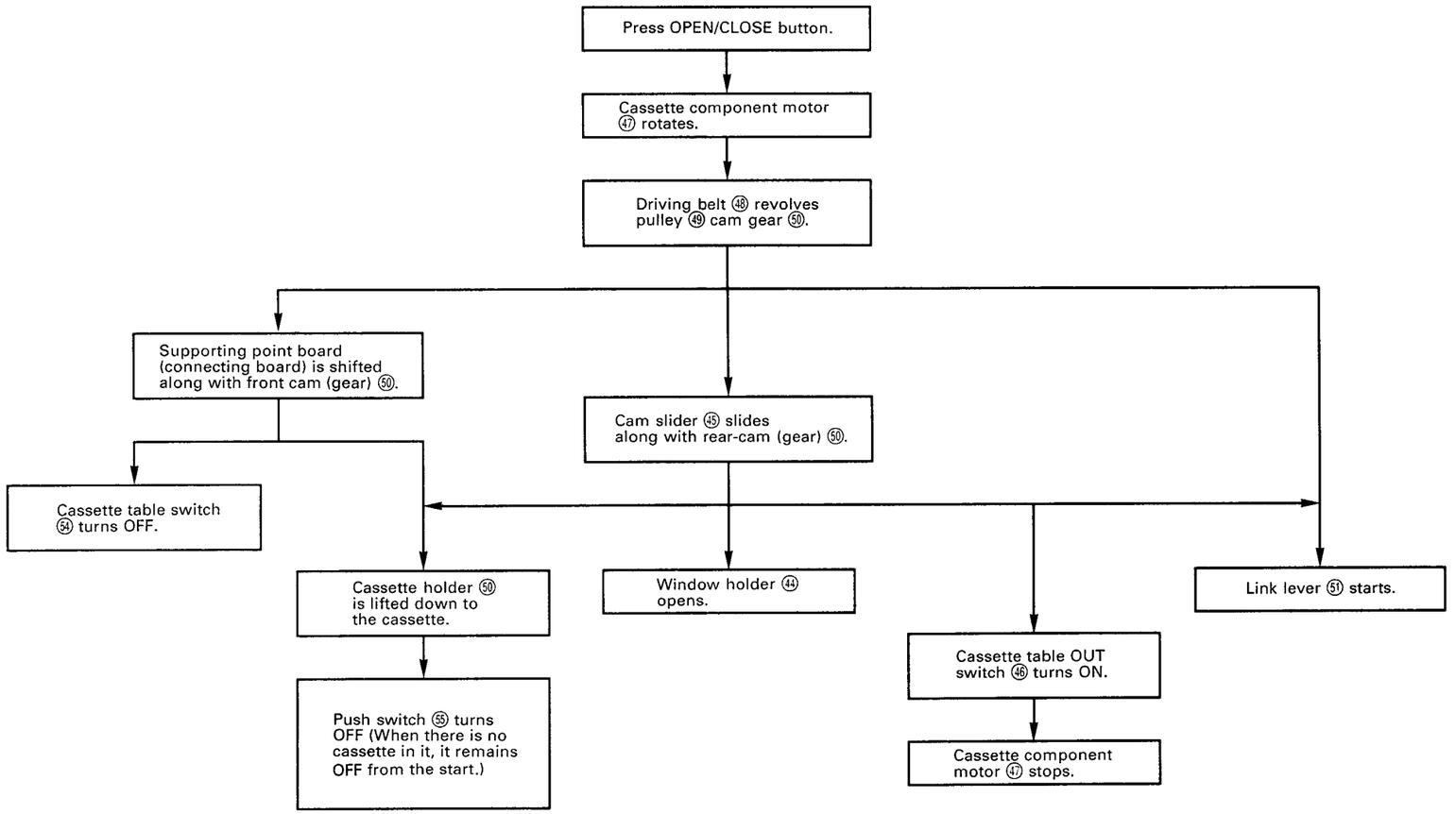
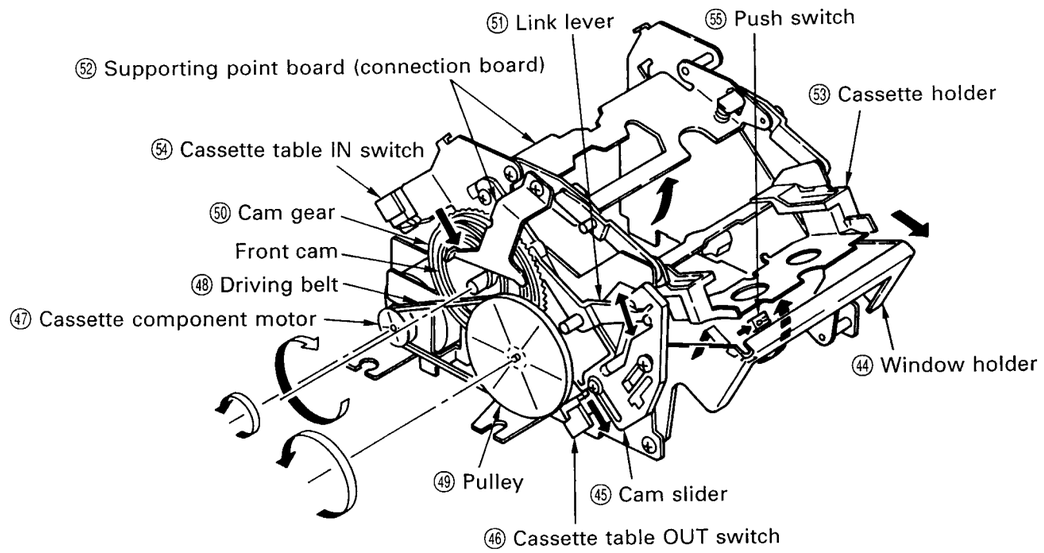


Fig. 9-27

9-2-10 EJECT





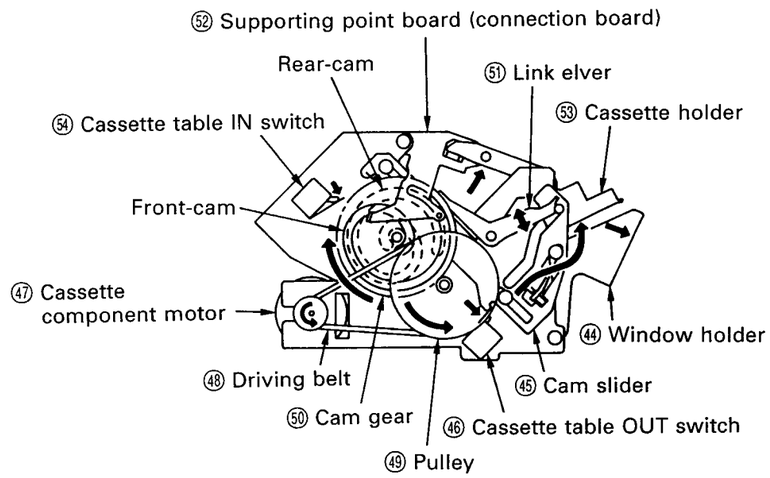
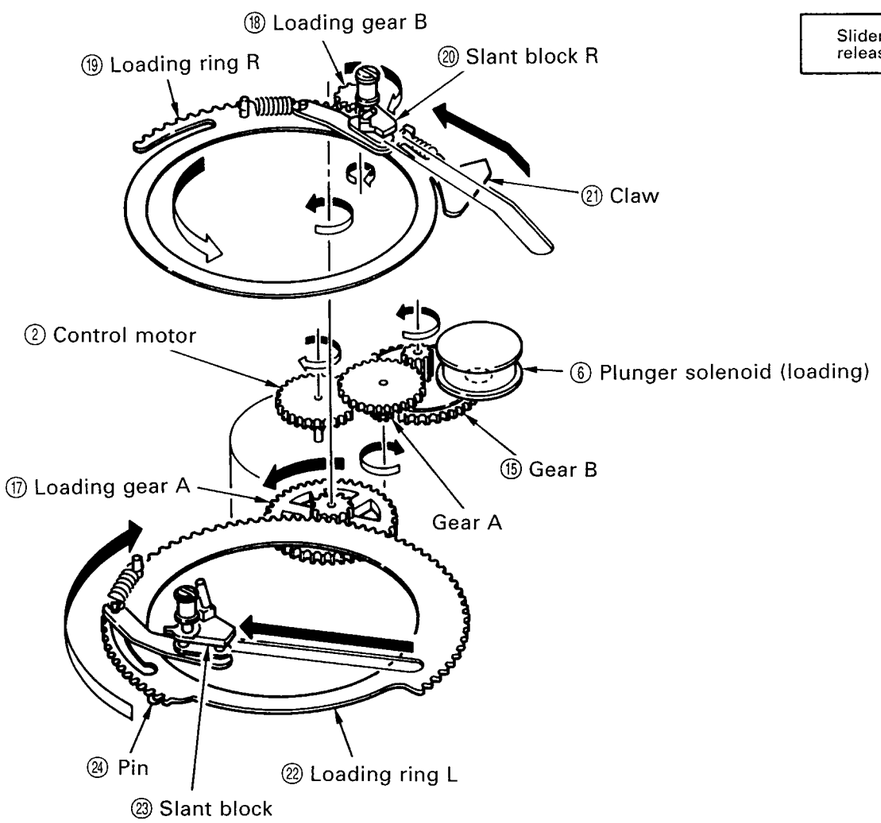
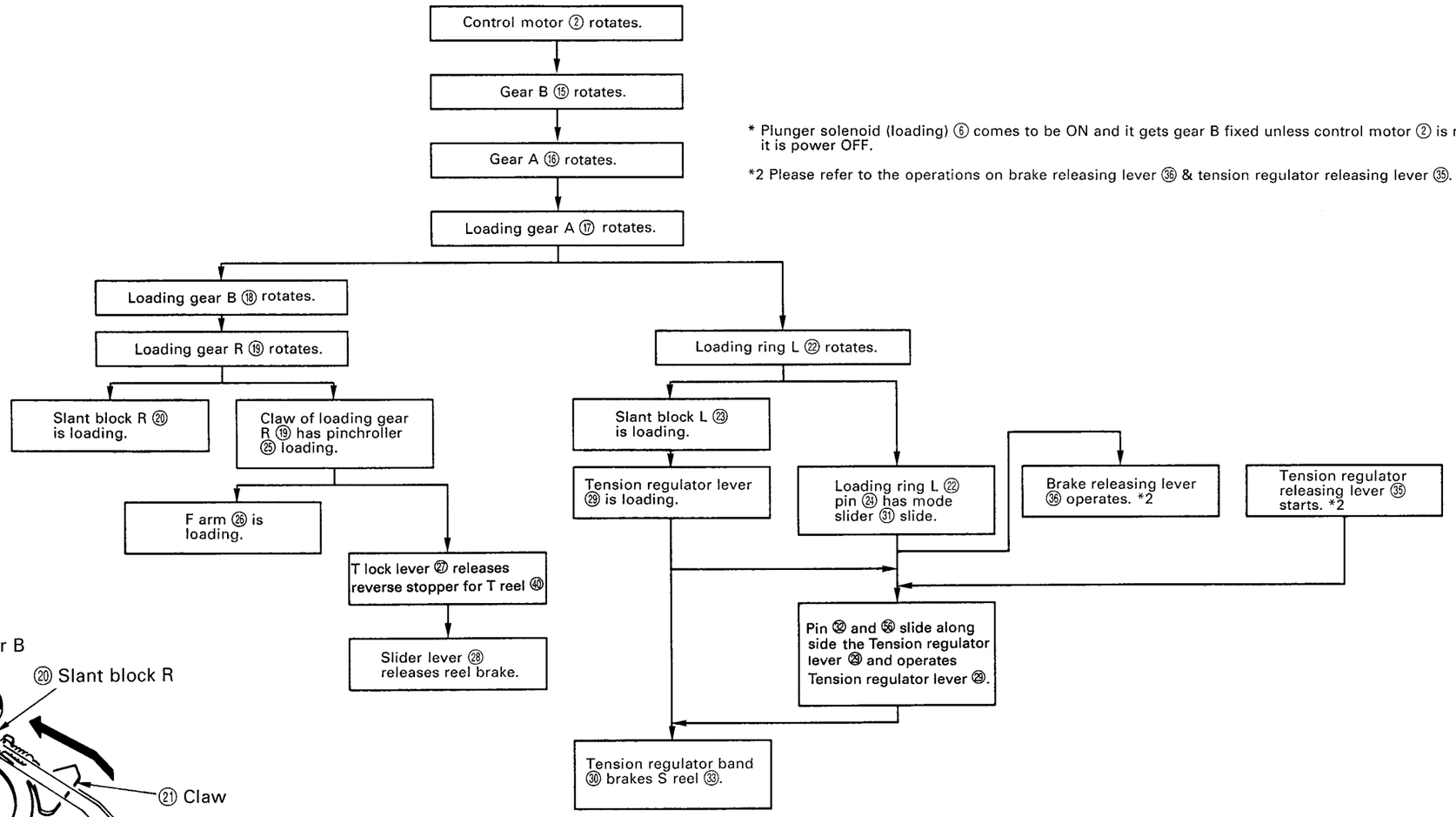


Fig. 9-28

9-3 Each Operation

9-3-1 Guide operation





* Plunger solenoid (loading) ⑥ comes to be ON and it gets gear B fixed unless control motor ② is rotating or it is power OFF.

*2 Please refer to the operations on brake releasing lever ㊱ & tension regulator releasing lever ㉟.

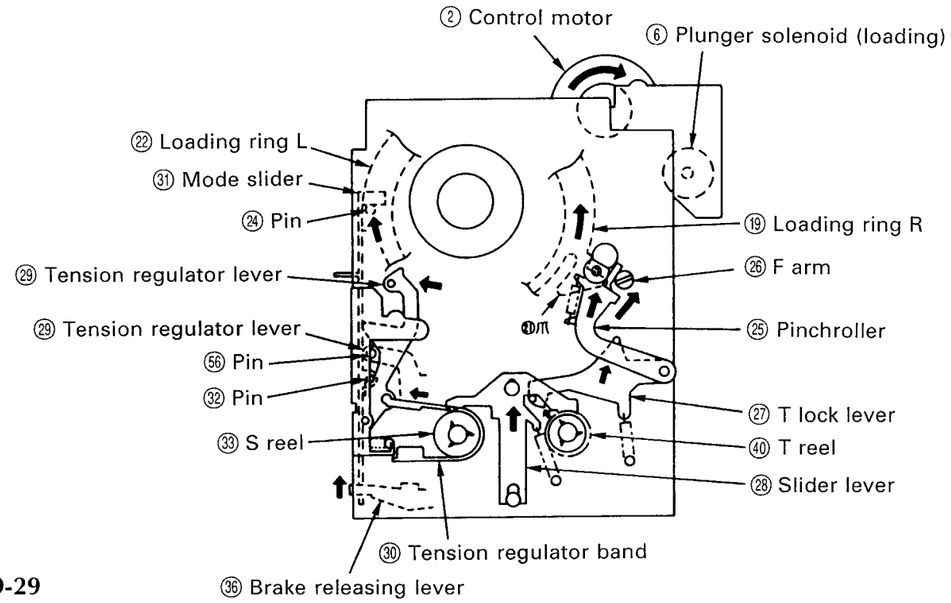
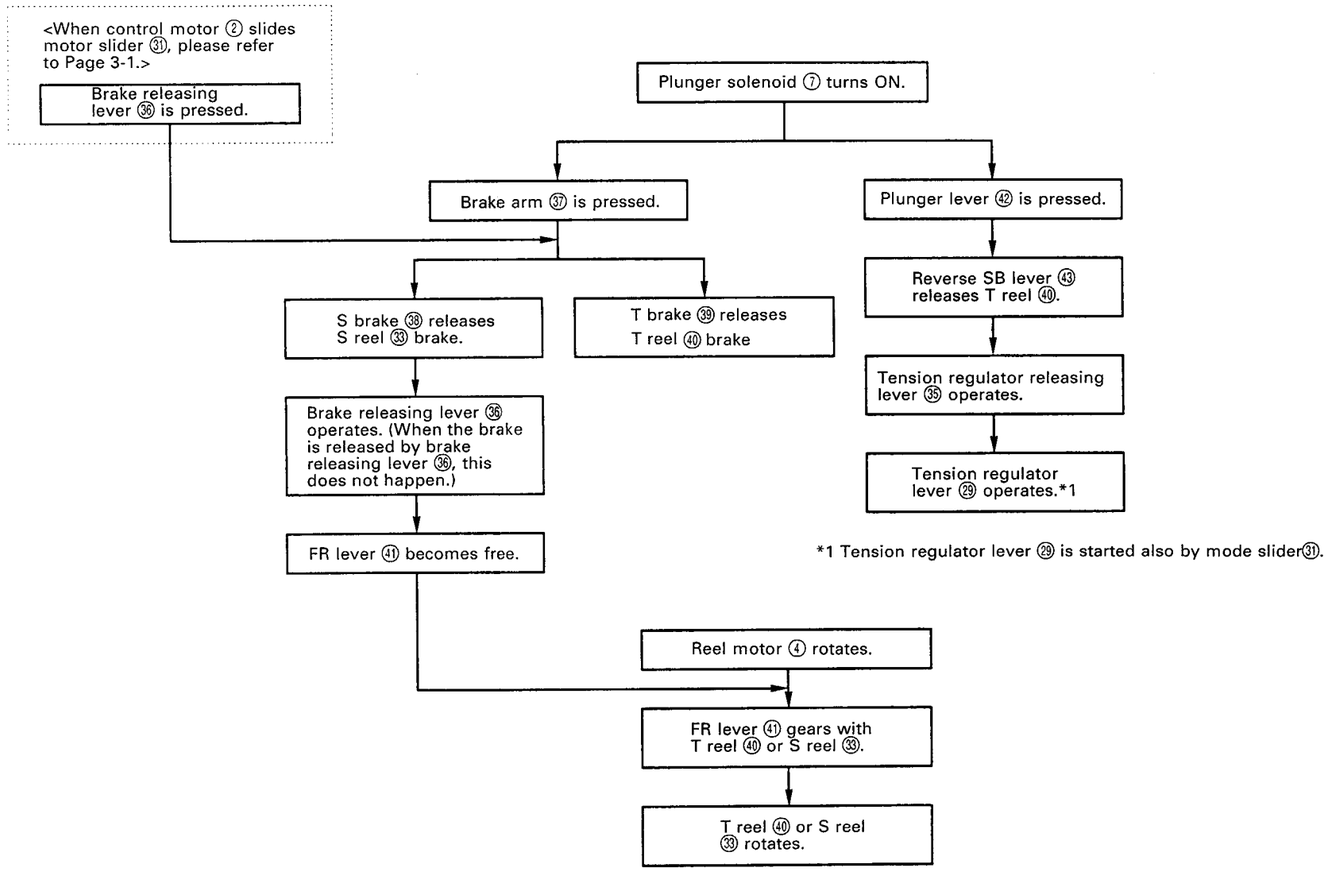
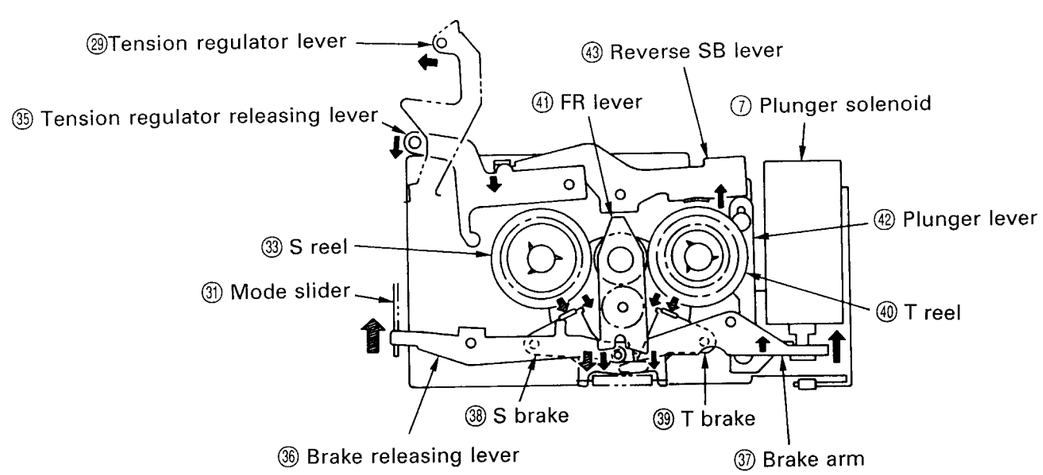


Fig. 9-29

9-3-2 Reel - board operation





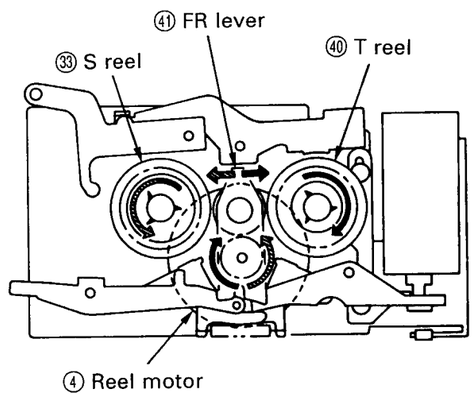


Fig. 9-30